Linear Integrated Circuits Applications

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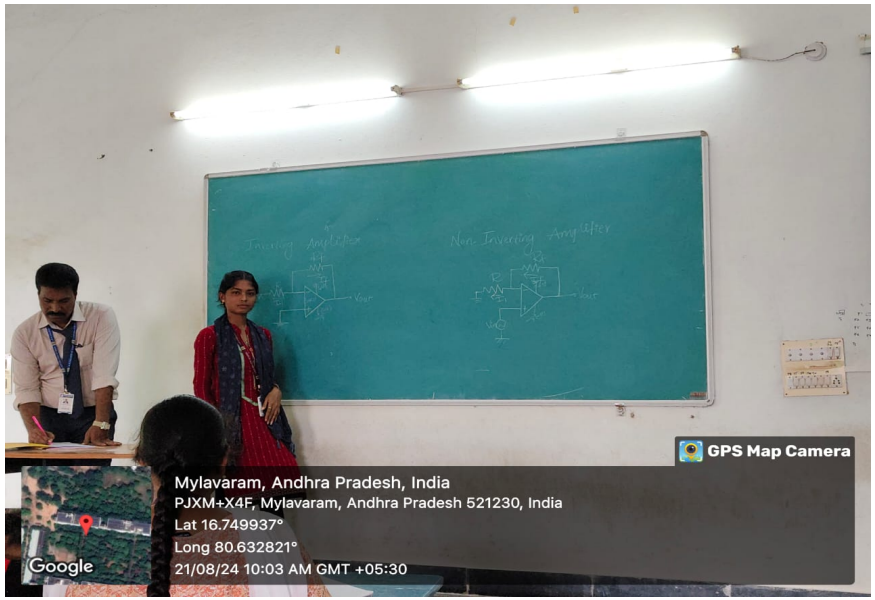

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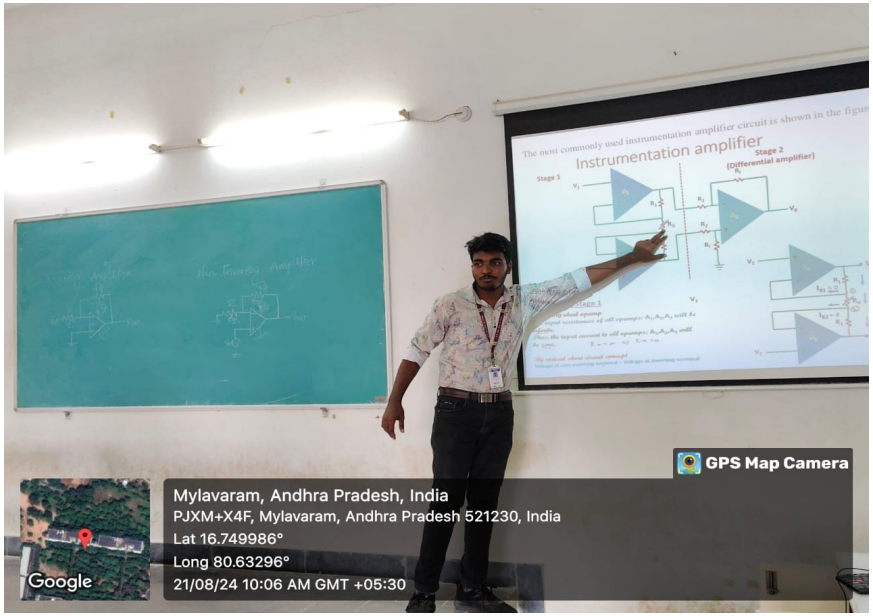

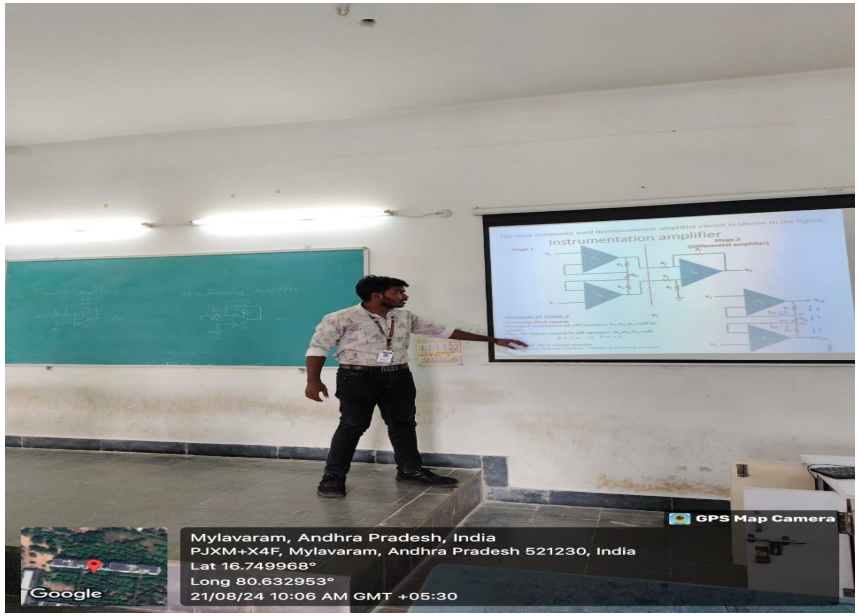

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20EC11 – LINEAR IC APPLICATIONS

Course Educational Objective: This course provides knowledge on Integrated Circuit (IC), Op-amp internal structure and various applications of it; Design of Op-Amp based Active Filters and waveform generators, applications of 555 timers and Phased Locked Loop.

Course Outcomes: At the end of the course, the student will be able to
CO1: Identify the building blocks of linear integrated circuits, characteristics and application of Op-Amps **(Understand – L2)**

CO2: Apply the concepts of feedback to op-amps for linear and non-linear applications **(Apply – L3)**

CO3: Analyze Op-Amp, 555 timer applications, phase locked loops to perform addition and multiplication of signals and voltage regulators using Linear ICs **(Analyze – L4)**

CO4: Design active filters, waveform generators and data converters using Op Amps **(Apply – L3)**

UNIT – I **[9 Hrs]**

Transistor Current Sources: Basic Current Source, Widlar Current Source, Cascode Current Source, Wilson Current Source.

Differential Amplifiers: Classification, DC and AC analysis of differential amplifier Configurations, specifications, FET differential amplifier, Level translator and current mirror circuit.

UNIT – II **[9 Hrs]**

Operational Amplifiers: Block Diagram, Ideal and Practical characteristics, DC and AC characteristics of Op-Amp, IC 741 specifications, Measurement of slew rate and CMRR.

Applications of OP Amps: Inverting and Non-inverting amplifier, Integrator and differentiator, Difference amplifier, Instrumentation amplifier, Analog multiplier, V to I, I to V converters, Rectifiers, Sample and Hold circuit, Log and Anti log amplifiers.

UNIT – III **[9 Hrs]**

Op Amp Active Filters: Design and analysis of 1st order & 2nd order Low pass and High pass filters, Band pass filter, Band reject filter and all pass filters.

Op Amp Waveform Generators: Comparator, design and analysis of Schmitt trigger, Astable, Monostable Multivibrators and Triangular wave Generator.

Op Amp Sine wave Oscillators: Design and analysis of RC Phase shift Oscillator, Wien Bridge Oscillator.

UNIT – IV **[8 Hrs]**

555 Timers: Functional Diagram, Monostable and Astable multivibrators and Applications, VCO - IC 566 & its features, IC 565 PLL Block Schematic, Applications of PLL.

IC Voltage Regulators: Fixed Voltage Regulators, IC723 General Purpose Regulator.

UNIT – V **[7 Hrs]**

Digital to Analog Converters: Weighted resistor DAC, R-2R Ladder DAC, Inverted R-2R DAC.

Analog to Digital Converters: Flash Type ADC, Counter Type ADC, Successive Approximation ADC, Charge Balancing ADC, Dual Slope ADC.

TEXT BOOKS

•Ramakanth A.Gayakwad, Op-amps and Linear Integrated Circuits, Third edition, PHI Publishers, 2006.

•Roy Choudhury D., Linear Integrated Circuits, Second edition, New Age International (P) Ltd.

REFERENCE

•Adel S. Sedra and Kenneth Carless Smith, Microelectronic Circuits, Fifth Edition. Oxford University Press.

•Rashid M. H., Microelectronic Circuits: Analysis and Design, Second edition, PWS Publishing Company.

Linear Integrated Circuits are solid state analog devices that can operate over a continuous range of input signals. Theoretically, they are characterized by an infinite number of operating states. Linear Integrated Circuits are widely used in amplifier circuits.

A simple electronic circuit can be designed easily because it requires few discrete electronic components and connections. However, designing a complex electronic circuit is difficult, as it requires more number of discrete electronic components and their connections.

It is also time taking to build such complex circuits and their reliability is also less. These difficulties can be overcome with Integrated Circuits.
The growth of any industry like communication, Control, instrumentation or computer is dependent on electronics. Integrated circuits are electronics.

Integrated Circuit (IC)

It is an **electronic circuit** is a group of electronic components connected for a specific purpose.

Integrated Circuit (IC) is a miniature , low cost electronic circuit, in which active (Diodes, Transistors etc) and passive (R,L,C) components are interconnected (Embedded) on a single chip of semiconductor material to perform various operations.

Advantages of integrated circuits

1. Miniaturization and hence increased equipment density.
2. Cost reduction due to batch processing.
3. Increased system reliability due to the elimination of soldered joints.
4. Improved functional performance.
5. Matched devices.
6. Increased operating speeds.
7. Reduction in power consumption

Depending upon the number of active devices per chip,there are different levels of integration

	Level of integration	Number of active devices per chip
1	Small scale integration(SSI)	Less then100
2	Medium Scale integration(MSI)	100-10000
3	Large scale integration(LSI)	1000-100,000
4	Very Large scale integration(VLSI)	Over 100,000
5	Ultra Large scale integration(ULSI)	Over 1 milloin

Applications:

Integrated circuits (IC) have revolutionized the world of electronics. They are used in virtually all electronic equipment today in applications including audio and radio communication, medical electronics and instrumentation control. Computers, mobile phones and other digital home appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of integrated circuits.

Based on fabrication Integrated Circuits are classified as

1. Monolithic ICs :Bipolar and Unipolar 2. Thick and Thin film ICs 3. Hybrid ICs

IC Package Types

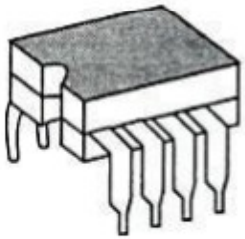
The op-amp ICs are available in various packages. The IC packages are classified as,

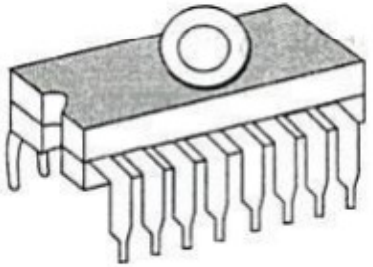
1.Metal Can

2.Dual In Line

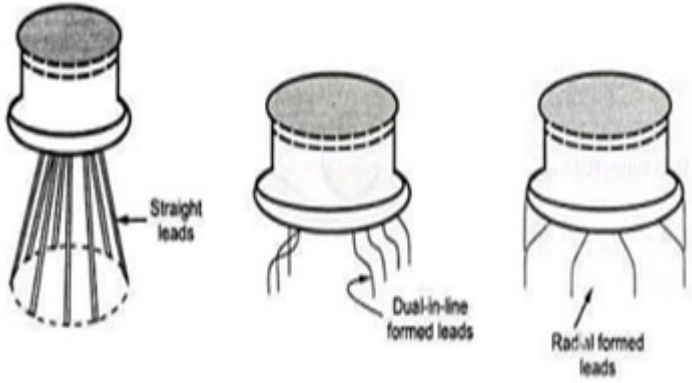
3.Flat Pack

n- Line Package:

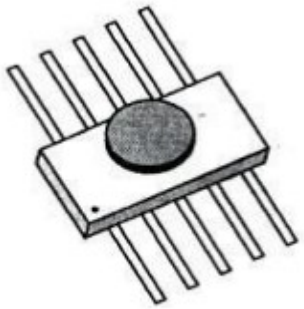




Metal Can



Flat Pack:

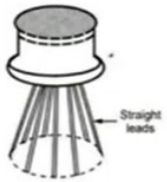


10 lead version

INTERNAL CIRCUIT :

Metal Can Packages

- Available in 3,5,8,10 & 12 pins.
- Also called Transistor pack.
- Plane is effective for heat dissipation, hence used in Power amplifiers.



Flat Package

- Used in the circuits where space is critical.
- Chip is enclosed in a rectangular ceramic case.
- Terminals taken out through the sides and ends.

Dual-in-Line Package

- Popular for commercial applications.
- Chip mounted inside a plastic or ceramic case.
- Easy to handle & mount, widely used.
- Available with 12,14,16,20,40 pins etc.,
- 8 pin Dip is called Mini-DIP

Advantages of Integrated Circuits:

Integrated circuits offer many advantages. They are discussed below −

Compact size- Miniaturization and hence increased equipment density. − For a given functionality, you can obtain a circuit of smaller size using ICs, compared to that built using a discrete circuit.

Lesser weight − A circuit built with ICs weighs lesser when compared to the weight of a discrete circuit that is used for implementing the same function of IC. using ICs, compared to that built using a discrete circuit.

Low power consumption − ICs consume lower power than a traditional circuit, because of their smaller size and construction.

Reduced cost − ICs are available at much reduced cost than discrete circuits because of their fabrication technologies and usage of lesser material than discrete circuits.

Increased reliability − Since they employ lesser connections, ICs offer increased reliability compared to digital circuits.

Improved operating speeds − ICs operate at improved speeds because of their switching speeds and lesser power consumption.

Types of Integrated Circuits:

Integrated circuits are classified as **Analog Integrated Circuits, Digital Integrated Circuits and Mixed Signal ICs**.

Analog Integrated Circuits:

Integrated circuits that operate over an entire range of continuous values of the signal amplitude are called as **Analog Integrated Circuits.** Analog Ics such as Sensors, Power management circuits and operational amplifiers are process analog signals. They perform amplification, filtering, Demodulation, Mixing etc.

These are further classified into the two types as discussed here −

Linear Integrated Circuits − An analog IC is said to be Linear, if there exists a linear relation between its voltage and current. IC 741, an 8-pin Dual In-line Package (DIP)op-amp, is an example of Linear IC.

Radio Frequency Integrated Circuits − An analog IC is said to be Non-Linear, if there exists a non-linear relation between its voltage and current. A Non-Linear IC is also called as Radio Frequency IC.

Digital Integrated Circuits:

It contains million of logic gates, Flip flops, Multiplexer, other circuits in a few square millimeters.

Small size of these circuits allow high speed, low manufacturing cost, low power consumption.

Digital Ics are microprocessors, DSPs, Microcontrollers and these are process zero(0) or One(1).

Current source:

Current source provides current to external circuit.
Current sink receives current from the external circuit.

A current source is a source that maintains the current at a particular value almost independent of the load conditions. The current source is a simple circuit, which will provide a current which remains constant independent of the load placed at its output.

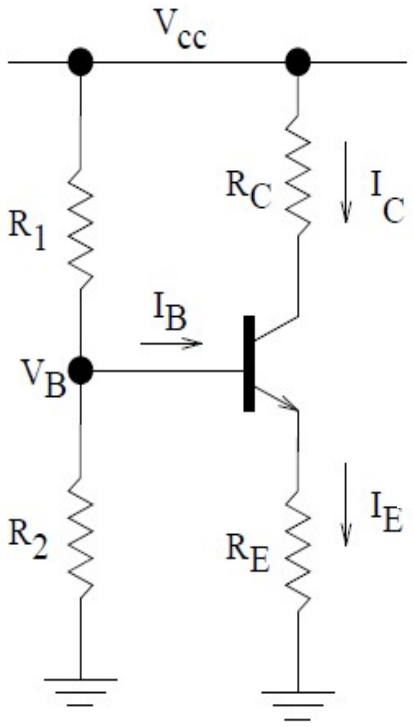
Active current sources using transistors are able to ***provide a much more constant current, or controlled current****.*

It is possible to make an active constant current source using a single transistor and a couple of resistors, although more comprehensive designs are also available using a few additional electronic components

A theoretical constant current source will be able to provide the constant current totally regardless of the impedance. Problems can occur when very high impedance levels or even open circuits are encountered because very high voltages might be required to reach the current levels required.

Transistor Current Source

Figure illustrates the basic configuration for a single-transistor current source. V_{CC} is a constant positive voltage from a DC power supply. Hence, the base voltage V_B is also a constant, with V_B = VCC*R2/(R1 +R2). R_L or R_C represents a load which we intend to power with a current which is approximately independent of the specific value of RL.



When the transistor is on, we have $I_E = (\beta+1)I_B$. In addition, we have $V_E = V_B - 0.6$; and $V_E = I_E * R_E = (\beta + 1)IB*RE$. Solving for I_B in this last equation gives $I_B = V_E/((\beta + 1)R_E)$.
We can combine these to solve for the current which passes through RL:

$$I_L = I_C = \beta I_B = \beta \frac{V_E}{(\beta+1)R_E} = \frac{\beta}{\beta+1}\frac{V_B - 0.6}{R_E} \approx \frac{V_B - 0.6}{R_E}$$

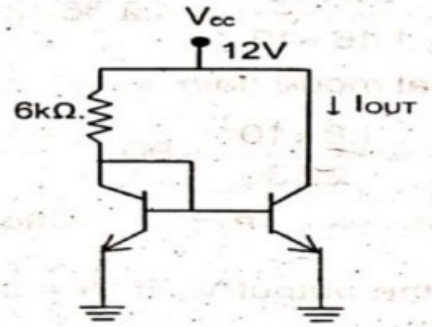
Hence, we see that indeed I_L is independent of R_L.

Basic transistor current source

Of course, there are limitations to the range of R_L for which the current source behaviour is reasonable. Recall that the transistor will shut down if $V_B \leq V_E$ or if V_{CE} is less than ≈ 0.2 V. These criteria determine the compliance of the current source, that is its useful operating range. So, for example, if we have $V_{CC} = 15$ V and $V_B = 5$ V in our circuit above, then $V_E = 5 - 0.6 = 4.4$ V, and the range of compliance for the collector voltage V_C will be approximately 4.6 V to 15 V.

GATE questions

1. A constant current source using two matched npn transistors with $\beta = 100$ and $V_{BE} = 0.6V$ is shown. Calculate I_{out}



(A) 1.5mA (B) 0.2mA
(C) 1.86mA (D) 2mA

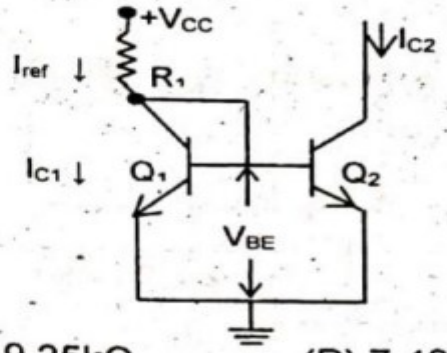
Sol. $I_{ref} = \frac{V_{CC} - V_{BE}}{R}$

$I_{ref} = \frac{12 - 0.6}{6K} = \frac{11.4}{6K} = 1.9mA$

$I_{OUT} = \frac{\beta}{2+\beta} I_{ref}$

$= \frac{100}{102} \times 1.9mA = 1.86mA$ Choice (C)

2. A current mirror shown below, provide a 1.5mA current with $V_{CC} = 12V$. Assume $\beta = 150$ and $V_{BE} = 0.7$volts. What is R_1.



(A) 9.25kΩ (B) 7.43kΩ
(C) 7.53kΩ (D) 8.5kΩ

Sol. $I_{C1} = I_{C2} = I_C$

$I_C = \frac{\beta}{\beta+2} I_{ref}$

$\Rightarrow I_C = \left(\frac{\beta}{\beta+2}\right) \times \frac{(V_{CC} - V_{BE})}{R_1}$

$\Rightarrow 1.5 \times 10^{-3} = \frac{150}{152} \times \frac{(12-0.7)}{R_1}$

$R_1 = \frac{11.15}{1.5} K\Omega = 7.43K\Omega$ Choice (B)

Operational Amplifier:

Operational Amplifier, also called as an Op-Amp, is an integrated circuit, which can be used to perform various linear, non-linear, and mathematical operations. An op-amp is a **direct coupled high gain amplifier**. You can operate op-amp both with AC and DC signals.

Construction of Operational Amplifier:

An op-amp consists of differential amplifier(s), a level translator and an output stage. A differential amplifier is present at the input stage of an op-amp and hence an op-amp consists of **two input terminals**. One of those terminals is called as the **inverting terminal** and the other one is called as the **non-inverting terminal**. The terminals are named based on the phase relationship between their respective inputs and outputs.

Characteristics of Operational Amplifier:

The important characteristics or parameters of an operational amplifier:

- Open loop voltage gain
- Output offset voltage
- Common Mode Rejection Ratio
- Slew Rate

Open loop voltage gain:

The open loop voltage gain of an op-amp is its differential gain without any feedback path. Mathematically, the open loop voltage gain of an op-amp is

$$A_v = \frac{V_0}{V_1 - V_2}$$

Output offset voltage:

The voltage present at the output of an op-amp when its differential input voltage is zero is called as **output offset voltage.**

Common Mode Rejection Ratio:

Common Mode Rejection Ratio (**CMRR**) of an op-amp is defined as the ratio of the closed loop differential gain, A_d and the common mode gain, A_c.

Mathematically, CMRR can be represented as $$CMRR = \frac{A_d}{A_c}$$

Note : the common mode gain, A_c of an op-amp is the ratio of the common mode output voltage and the common mode input voltage.

Slew Rate:

Slew rate of an op-amp is defined as the maximum rate of change of the output voltage due to a step input voltage.

Mathematically, slew rate (SR) can be represented as −

$$Slew\ Rate = \frac{dv_0}{dt}$$

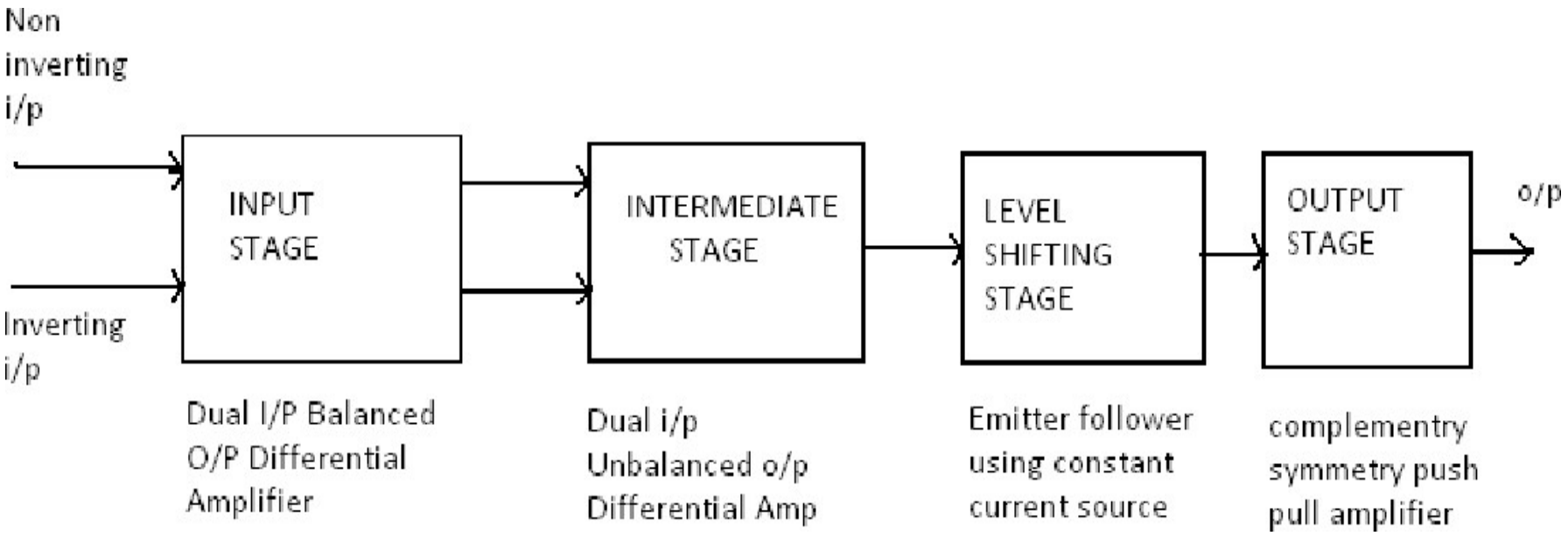
Where, V_0 is the output voltage. Slew rate is measured in V/ μsec or V/ msec.

Operational amplifier:

The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MHz to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency.

The internal block diagram of an op-amp is shown in the fig The input stage is the dual input balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp.

The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. On most amplifiers, the intermediate stage is dual input, unbalanced output. Because of direct coupling, the dc voltage at the output of the intermediate stage is well above ground potential.

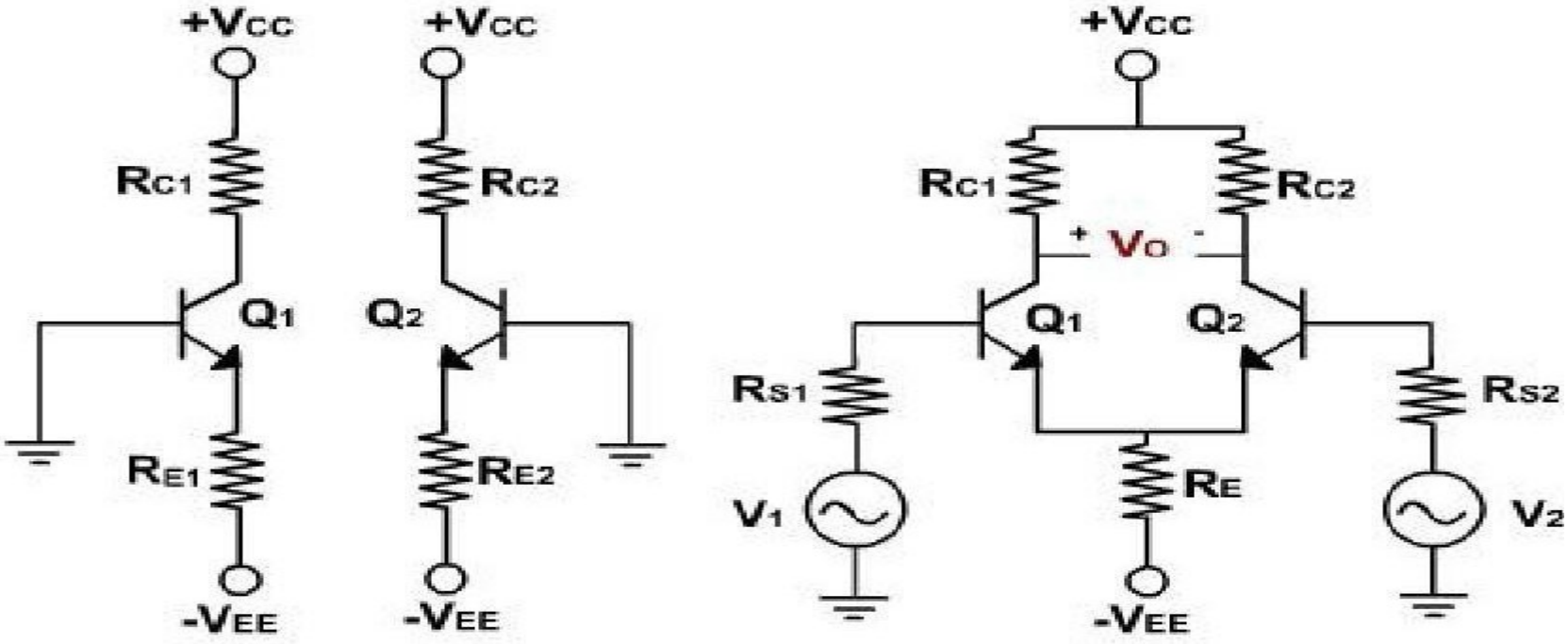


Therefore, the level translator (shifting) circuit is used after the intermediate stage downwards to zero volts with respect to ground.

The final stage is usually a push pull complementary symmetry amplifier output stage. The output stage increases the voltage swing and raises the ground supplying capabilities of the op-amp. A well designed output stage also provides low output resistance.

Differential amplifier:

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals.
The two transistors Q1 and Q2 have identical characteristics.
The resistances of the circuits are equal, i.e. RE1 = R E2, RC1 = R C2 and the magnitude of +VCC is equal to the magnitude of -VEE. These voltages are measured with respect to ground.



Differential amplifier

To make a differential amplifier, the two circuits are connected as shown in fig. The two +VCC and -VEE supply terminals are made common because they are same.

The two emitters are also connected and the parallel combination of RE1 and RE2 is replaced by a resistance RE.

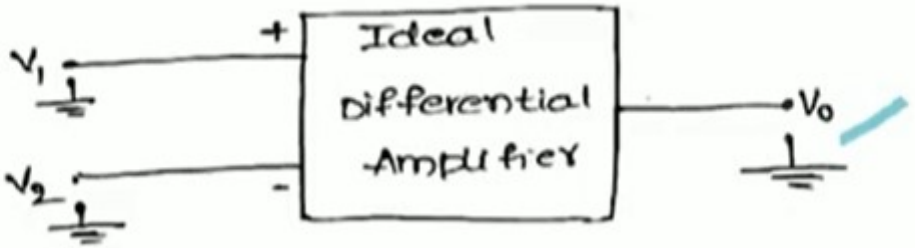
The two input signals v1& v2 are applied at the base of Q1 and at the base of Q2. The output voltage is taken between two collectors.

The collector resistances are equal and therefore denoted by RC = RC1 = RC2.

Ideally, the output voltage is zero when the two inputs are equal.
When v1 is greater then v2 the output voltage with the polarity shown appears.
When v1 is less than v2, the output voltage has the opposite polarity.

Differential Amplifier

- It is the basic building block of Op Amp.
- It amplifies the difference between two input voltage signals and rejects the common mode signals.



- In ideal differential amplifier, the output voltage is proportional to difference of two input voltage signals.

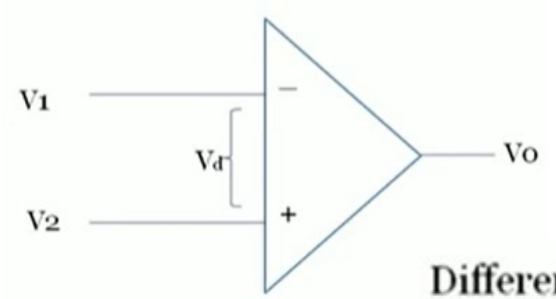
$$V_o \propto (V_1 - V_2) \rightarrow ①$$

- Differential amplifier operates in two modes.

1. Differential Mode of operation → >>> Two input signals are different.
2. Common Mode of operation → >>> Two input signals are same.

Differential Mode gain, Ad

Differential mode→ Vin1≠Vin2

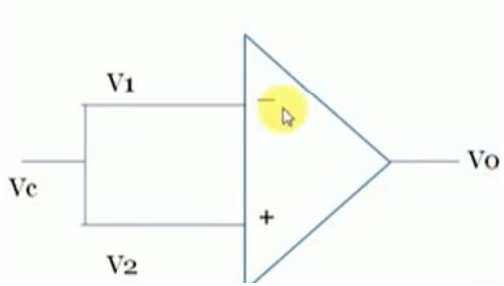


$V_o = A_d V_d$ Where Vd=V2-V1

Differential mode gain, $A_d = \frac{V_o}{V_d}$

Differential mode gain in dB, $A_d = 20 \log_{10}\left(\frac{V_o}{V_d}\right)$ in dB

Common Mode gain, Ac



Common mode→ Vin1=Vin2

$V_o = A_c V_c$

Where $V_c = \frac{V_1+V_2}{2}$ Average of two input signals

Common mode gain, $A_c = \frac{V_o}{V_c}$

Common mode gain in dB, A_c (in dB) $= 20 \log \left(\frac{V_o}{V_c}\right)$

Finally, the total output of differential amplifier is

Vo=Vo(differential mode)+Vo(common mode) $V_o = V_d A_d + V_c A_c$

Common mode Rejection Ratio (CMRR):

- The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called Common Mode Rejection Ratio.
- Mathematically, CMRR is defined as the ratio of differential voltage gain to common mode voltage gain.

$$CMRR, \rho = |Ad/Ac|$$

$$\text{CMRR in dB} = 20 \log \left| \frac{A_d}{A_c} \right| \text{ dB}$$

The output voltage, V_o can be expressed interms of CMRR as below: We know that, $V_o = V_d A_d + V_c A_c$

$$V_o = A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d}\right)$$

$$V_o = A_d V_d \left[1 + \frac{1}{\rho} \cdot \frac{V_c}{V_d}\right]$$

$V_o = A_d V_d$ For higher values of ρ

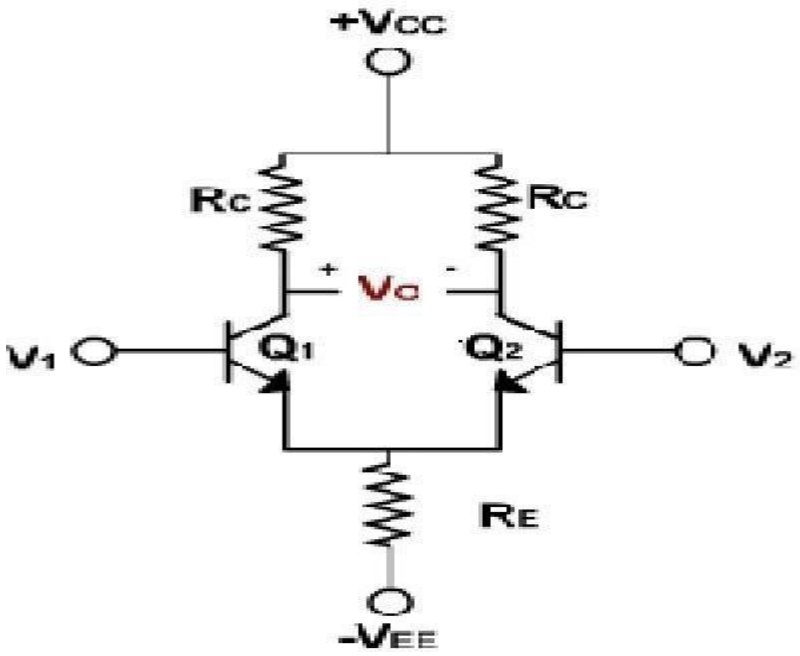
The differential amplifiers are of different configurations.

The four differential amplifier configurations are following:

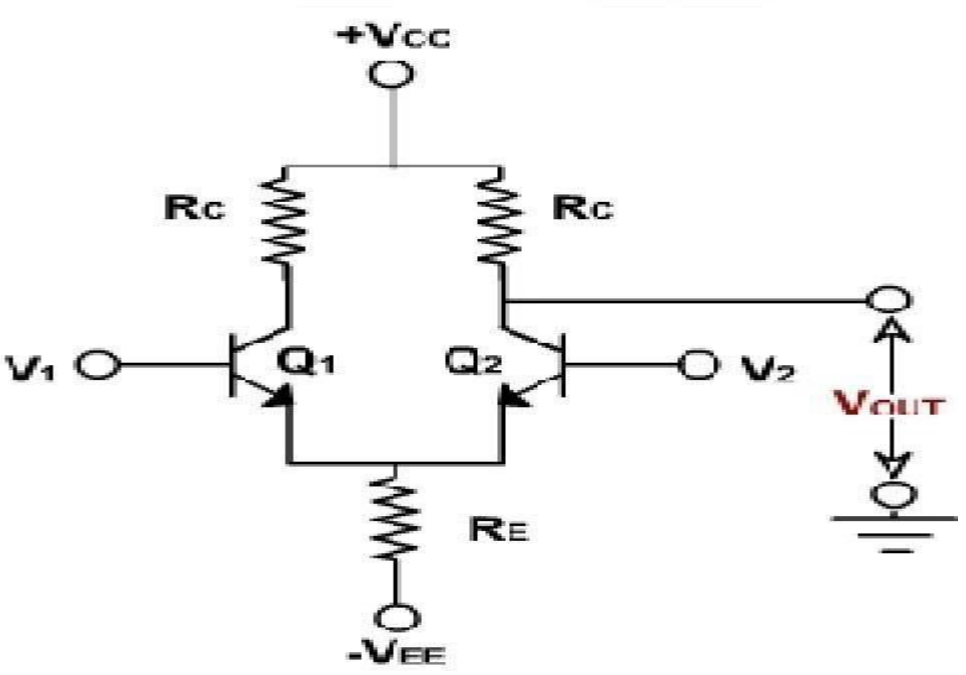
1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
3. Single input balanced output differential amplifier.
4. Single input unbalanced output differential amplifier.

These configurations are shown in fig and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

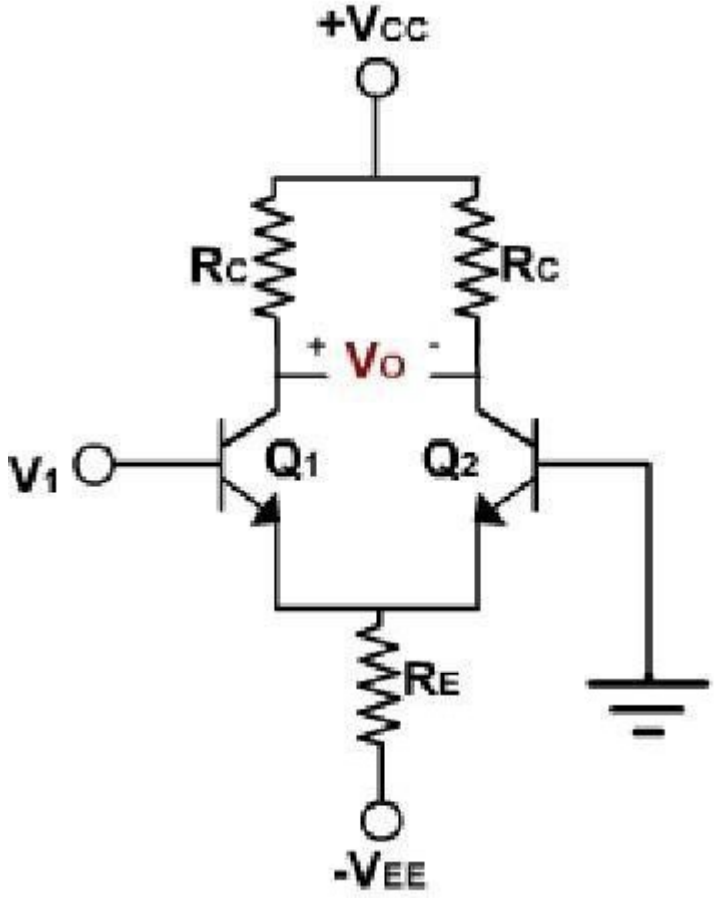
A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.



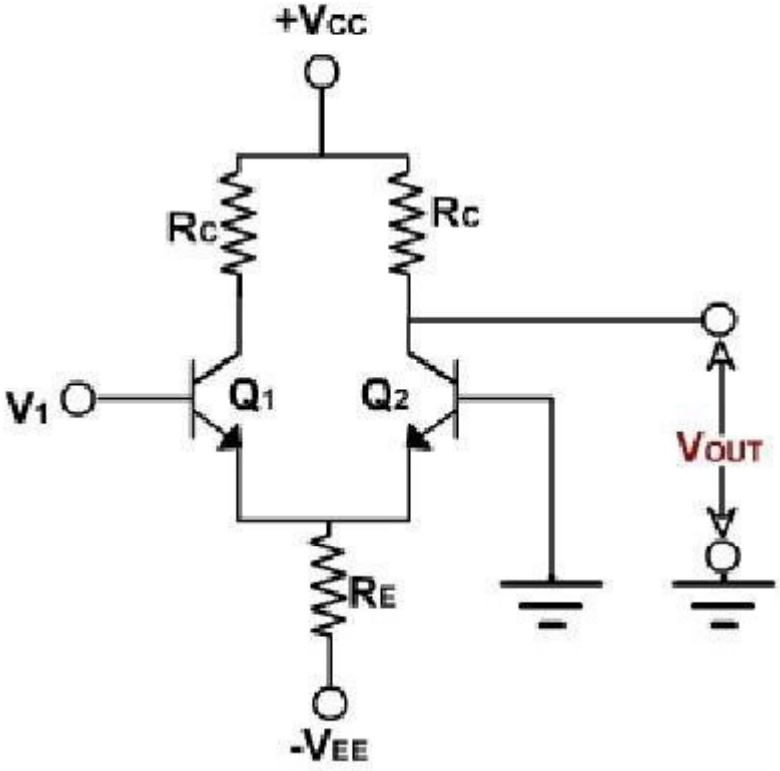
Dual input, balanced output differential amplifier.



Dual input, unbalanced output differential amplifier.



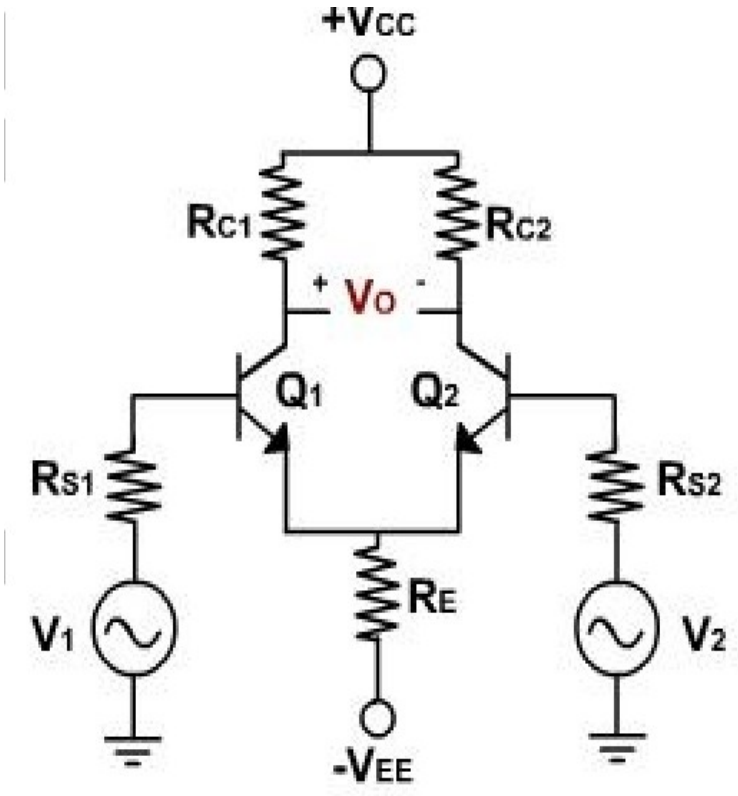
Single input, balanced output differential amplifier

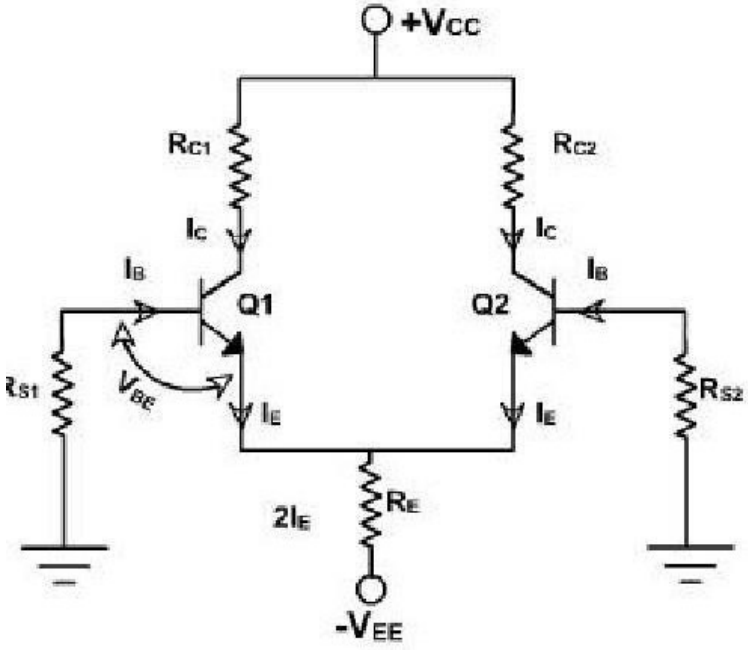


Single input, unbalanced output differential amplifier.

Dual Input, Balanced Output Differential Amplifier:

The circuit is shown in figV1 and V2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2, which are at same dc potentials.





D.C. Analysis:

To obtain the operating point (ICQ and VCEQ) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages V1 and V2 to zero as shown in fig

The internal resistances of the input signals are denoted by R_S because RS1= RS2. Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of ICQ and VCEQ can be used for second transistor Q2.
Applying KVL to the base emitter loop of the transistor Q1.

$$R_S I_B + V_{BE} + 2 I_E R_E = V_{EE}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \qquad (E-1)$$

$V_{BE} = 0.6V$ for S_i and $0.2V$ for G_e.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

The value of R_E sets up the emitter current in transistors Q1 and Q2 for a given value of V_{EE}.
The emitter current in Q1 and Q2 are independent of collector resistance R_C.
The voltage at the emitter of Q1 is approximately equal to -VBE if the voltage drop across R_{Sin} is negligible. Knowing the value of IC the voltage at the collector VC is given by

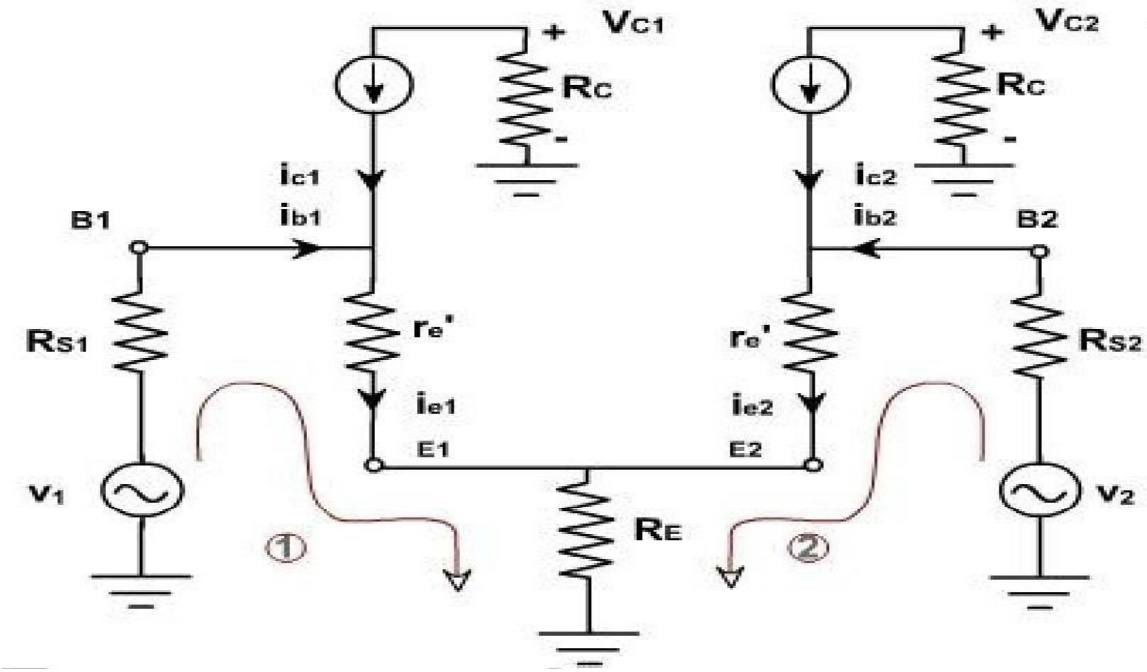
$$VC = VCC - IC\,RC \text{ and } VCE = VC - VE$$

$$= VCC - IC\,RC + VBE$$

$$VCE = VCC + VBE - ICRC$$

From the two equations VCEQ and ICQ can be determined. This dc analysis is applicable for all types of differential amplifier.

A.C. Analysis :



The circuit is shown in fig. V1 and V2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2, which are at same dc potentials.

Dc analysis has been done to obtain the operating point of the two transistors. To find the voltage gain Ad and the input resistance Ri of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown in fig. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.

The output voltage VO is given by

$$V_o = V_{c2} - V_{c1}$$
$$= -R_C i_{C2} - (-R_c i_{c1}$$
$$= R_C(i_{C1} - i_{c2})$$
$$= R_C(i_{e1} - i_{e2})$$

Substituting ie1, & ie2 in the above expression

$$V_o = R_C\left\{\frac{(r_e + R_E)V_1 - R_E V_2}{(r_e' + R_E)^2 - R_E^2} - \frac{(r_e + R_E)V_2 - R_E V_1}{(r_e' + R_E)^2 - R_E^2}\right\}$$

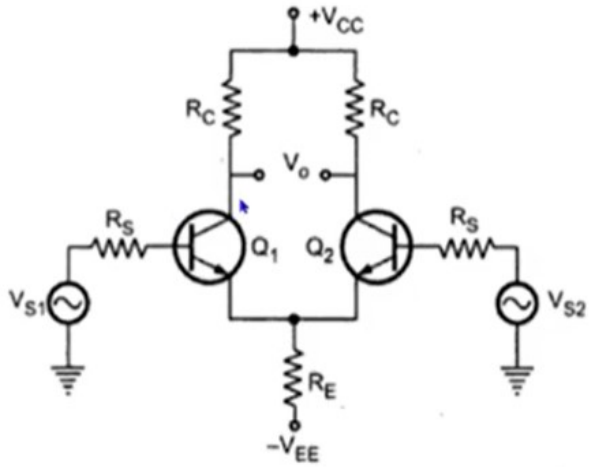
$$= \frac{R_C(V_1 - V_2)(r_e' - 2R_E)}{r_e'(r_e' + 2R_E)}$$

$$V_o = \frac{R_C}{r_e'}(V_1 - V_2) \ldots\ldots\ldots\ldots E(1)$$

Thus a differential amplifier amplifies the difference between two input signals. Defining the difference of input signals as Vd =V1 -V2 the voltage gain of the dual input balanced output differential amplifier can be given by (E-2)

Analysis of differential amplifiers using h-parameters:

Analysis of Differential Amplifier using h-parameters:



D.C analysis is same as r-parameter model

$$VC = VCC - IC\,RC \text{ and } VCE = VC - VE$$

$$= VCC - IC\,RC + VBE$$

$$VCE = VCC + VBE - ICRC$$

$$R_S\, I_B + V_{BE} + 2\, I_E\, R_E = V_{EE}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \qquad (E-1)$$

$V_{BE} = 0.6V$ for S_i and $0.2V$ for G_e.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

From the two equations VCEQ and ICQ can be determined. This dc analysis is applicable for all types of differential amplifier.

The following specifications are given for the dual input, balanced output differential amplifier R_c=2.2kΩ, R_E=4.7kΩ, R_{i1}=R_{i2}=50Ω, V_{CC}=10V,
-V_{EE}= -10V, β=100 and V_{BE}=0.715V
Determine 1) Voltage Gain 2) Input Resistance 3) Output Resistance

Solution:

r'e=Thermal Voltage/IE=25mV/IE

So at room temp (300K), this quantity kT/q (thermal voltage) works out to about 25.89mV. So if the temperature is less than 300K (27°C), it will be closer to 25mV.
Usually, I consider it 26mV.

- We know that the equations for operating point

$$IE \cong IcQ = \left[\frac{VEE - VBE}{2RE}\right]$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_C R_C$$

I_{CQ} = 0.988 mA
V_{CEQ}=8.54V

- b). The input resistance seen from each input source is given by (E-3) and (E-4):

$$R_{i1} = R_{i2} = 2\beta_{ac} r_e = (2)(100)(25.3) = 5.06k\Omega$$

- c) The output resistance seen looking back into the circuit from each of the two output terminals is given by (E-5)

$$R_{o1} = R_{o2} = 2.2\ k\ \Omega$$

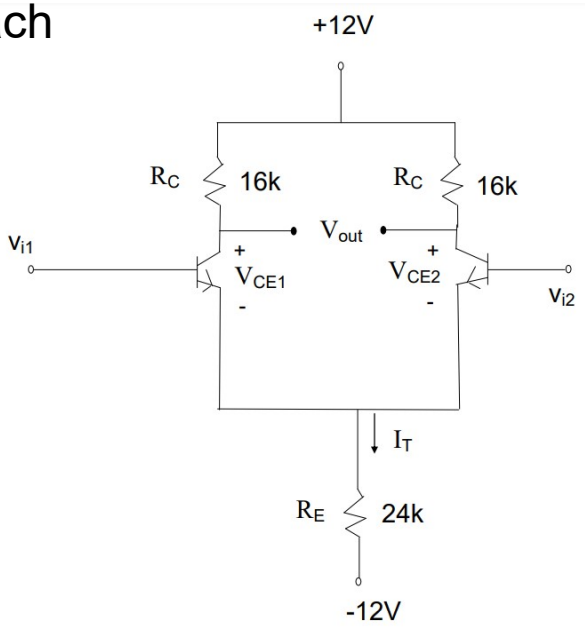
- The ac emitter resistance

$$r_e' = \frac{25mV}{I_E mA} = \frac{25mV}{0.988mA} = 25.3\Omega$$

- Therefore, substituting the known values in voltage gain equation (E-2), we obtain

$$A_d = \frac{v_o}{v_{id}} = \frac{R_C}{r_e} = \frac{2.2\,k\Omega}{25.3} = 86.96$$

Estimate dc emitter current in each transistor of differential amplifier shown in fig. How much is dc voltage from each collector to ground? How much is Vout?



$$I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

$I_C = I_E = \frac{12-0}{2\times24\times10^3} = 0.25\ mA.$ assume $V_{BE} = 0$

Since $I_C = I_E$, voltage summation in the output circuit gives,

$V_{CC} = I_C R_C + V_{CE1}$

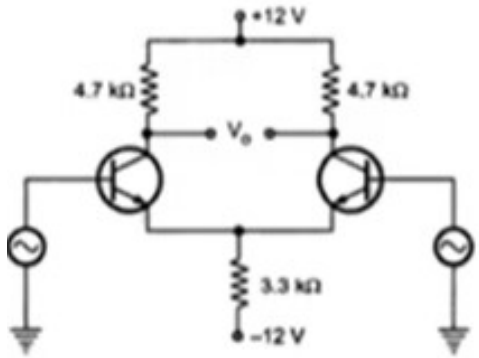
$V_{CE1} = V_{CC} - I_C R_C = 12 - 0.25X10^{-3} \times 16X10^3$

Or, $V_{CE1} = 8.0\ V = V_{CE2}$ (due to symmetry)

Then,

$V_{out} = V_{CE1} - V_{CE2} = 8 - 8 = 0V$

1. Calculate the operating pint values for the circuit



$$I_E = \frac{V_{EE} - V_{BE}}{2R_E}$$

$$= \frac{12 - 0.7}{2 \times 3.3 \times 10^3} = 1.712 \text{ mA}$$

$$I_C = I_E = 1.712 \text{ mA} \quad I_{CQ} = 1.712 \text{ mA}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

$$= 12 + 0.7 - 1.712 \times 10^{-3} \times 4.7 \times 10^3 = 4.653 \text{ V.}$$

2 .The common mode input to a certain differential amplifier, having differential gain of 125 is 4 Sin 200 ∏ t. Determine the common mode output if CMRR is 60dB.

- 60 = 20 Log (Ad/Ac)
- Log (Ad/Ac) = 3
- (Ad/Ac) = 1000 wkt Ad = 125
- Ac = Ad/1000 = (125/1000) = 0.125

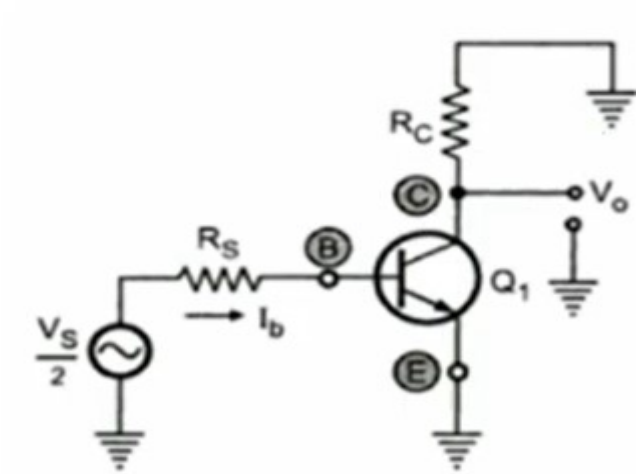
V_{oc} = Ac Vc = 0.125(4 Sin 200 ∏ t) = **0.5 Sin (200∏t) V**

3. An op-amp has a differential gain of 80dB and CMRR of 95dB. If V1 = 2uV and V2 =1.6uV, then calculate the differential and common mode output values.

- Ad in dB = 20 log Ad = 80
- Ad = 1×10^4
- CMRR in dB = 20 log CMRR
- 95 = 20 log CMRR
- CMRR = 5.6234×10^4
- Differential output can be calculated as
- Vd = Ad (V1 – V2)
- = $1 \times 10^4 (2-1.6) \times 10^{-6}$
- = 4mV

- The common mode output can be calculated as,
- Vc = Ac(V1+V2)/2
- CMRR = Ad/Ac
- $5.6234 \times 10^4 = (1 \times 10^4) /Ac$
- Ac = 0.1778
- Vc = $0.1778 \times (2+1.6)/ 2 \times 10^{-6}$
- Vc = 0.32uV

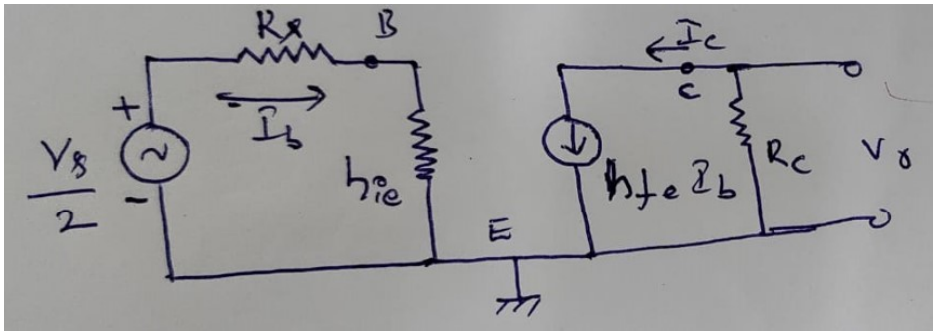
A.C. analysis • Differential Voltage gain (A_d



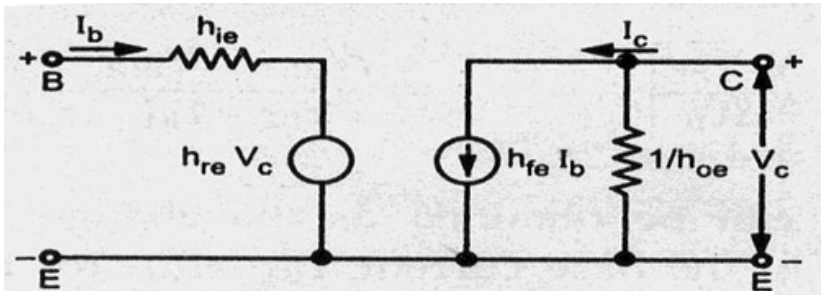
Actually a.c. input voltage is Vs, but we are considered one half of the differential amplifier, so the input a.c. Voltage should be Vs / 2.

The two inputs are same in magnitude and opposite in phase. Vs1=Vs2= Vs/2.

The two emitter currents ie1 & ie2 are equal in magnitudes and 180^0 out of phase. Hence they cancel each other.



H- parameter equivalent circuit



In approximation or Simplified model h_{oe} and h_{re} are neglected . Because

h_{oe} = 25 μA/V = 25 x 10^{-6} ≈ 0

h_{re} = 25 x 10^{-4} ≈ 0

- Apply KVL for input loop

$$-I_b R_s - I_b\, hie + \frac{Vs}{2} = 0 \quad \text{--- (1)}$$

$$-I_b\,(R_s + hie) = -\frac{Vs}{2}$$

$$I_b = \frac{Vs}{2(Rs + hie)} \quad \text{--- (2)}$$

Applying KVL to the output loop,

$$V_o = -\,hfe\, I_b\, R_c \quad \text{--- (3)}$$

Sub (2) in (3)

$$V_o = -\,hfe\, R_c \frac{Vs}{2(Rs + hie)}$$

$$\frac{V0}{Vs} = \frac{-\,hfe\, Rc}{2(Rs + hie)}$$

-ve sign indicate 180^0 phase differennce between input and output

The two input signal have magnitudes Vs/2

- Two input signal magnitudes are $V_s/2$

$$V_d = \frac{Vs}{2} - \left(-\frac{Vs}{2}\right) = V_s$$

$$A_d = \frac{V0}{Vs} = \frac{-\,hfe\,Rc}{2(Rs + hie)} \quad \text{(for unbalanced output)}$$

This unbalanced because output is measured w.r.t ground

- For Balanced output

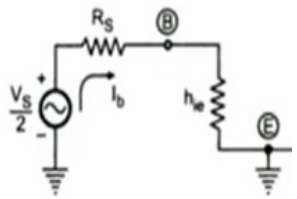
$$A_d = \frac{V0}{Vs} = 2\,X\,\frac{-\,hfe\,Rc}{2(Rs + hie)}$$

$$A_d = \frac{V0}{Vs} = \frac{-\,hfe\,Rc}{(Rs + hie)} \quad \text{(Balanced output)}$$

For balanced output is measured between two collectors.
Balanced output is double than unbalanced.

- **Differential Input impedance (R_i):**
  - It is the equivalent resistance measured between one of the input and the ground when other input is grounded.

$$R_i = \frac{Vs}{Ib}$$



Applying KVL to input loop

$$-I_bR_s - I_b\,hie + \frac{Vs}{2} = 0 \quad \text{--- (1)}$$

$$V_s = 2 * I_b\,(R_s + hie)$$

$$R_i = \frac{Vs}{Ib} = 2\,(R_s + hie)$$

Note: Input resistance doesn't depends on output, weather the output is balanced or unbalanced.

Note: In equivalent h-parameter circuit, output is measured between collector and ground, hence the analysis is unbalanced.

Output Resistance (R_o) :

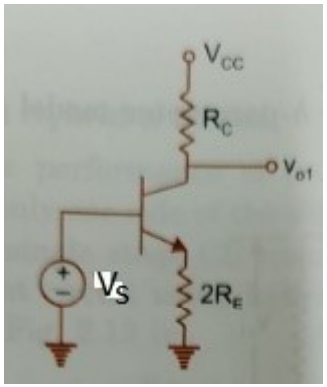
- It is defined as the equivalent resistance measured between one of the output terminals with respect to the ground.

$$R_o = R_C$$

Common mode gain(A_c):

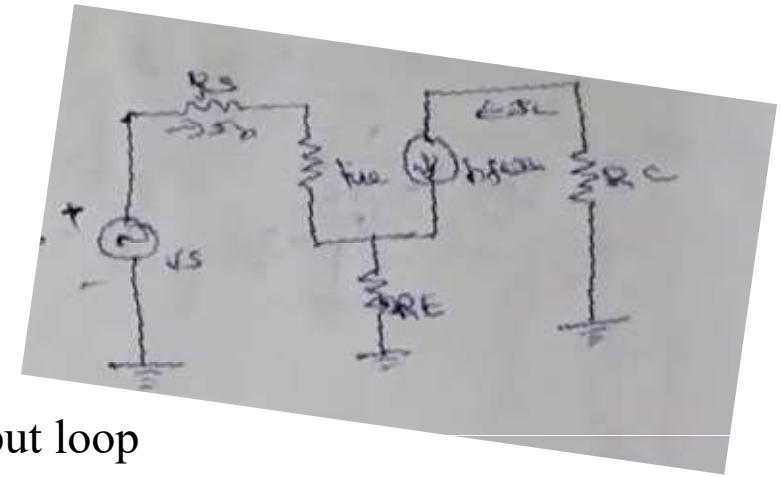
In common mode, V_1 and V_2 are increased by Incremental voltage (common mode)V_c. Both the collector curents ic_1 &ic_2 will increase by incremental current ic. The current through RE now increases by $2i_e$. To draw the common mode half circuit, replace the RE by $2R_E$.

$$V_c = (V_1+V_2)/2 = (V_s+V_s)/2 = 2V_s/2 = V_s$$



Common-mode half circuit

$$V_0 = A_C V_S \qquad A_C = V_0 / V_S$$



KVL for input loop

$$V_S - I_b R_s - h_{ie} I_b - 2R_E I_E = 0$$

$$V_s = I_b R_s + I_b h_{ie} + 2R_E (1+h_{fe} I_b)$$

$$V_s = I_b [R_s + h_{ie} + 2R_E (1+h_{fe})]$$

$$V_o = -I_c R_c \Rightarrow -h_{fe} I_b R_c$$

$$A_c = \frac{-h_{fe} R_c}{R_s + h_{ie} + 2R_E (1+h_{fe})}$$ ⇒ both balanced & unbalanced o/p.

$$A_c = \frac{V_o}{V_s} = \frac{-h_{fe} I_b R_c}{I_b (R_s + h_{ie} + 2R_E (1+h_{fe}))}$$

CMRR :

$$CMRR = 20 \log \left| \frac{A_d}{A_c} \right|$$

$$CMRR = 20 \log \left| \frac{R_s + h_{ie} + 2R_E(1+h_{fe})}{R_s + h_{ie}} \right| \Rightarrow dB \text{ for balanced o/p}$$

$$= 20 \log \left| \frac{R_s + h_{ie} + 2R_E(1+h_{fe})}{2(R_s + h_{ie})} \right| dB \Rightarrow \text{Unbalanced o/p.}$$

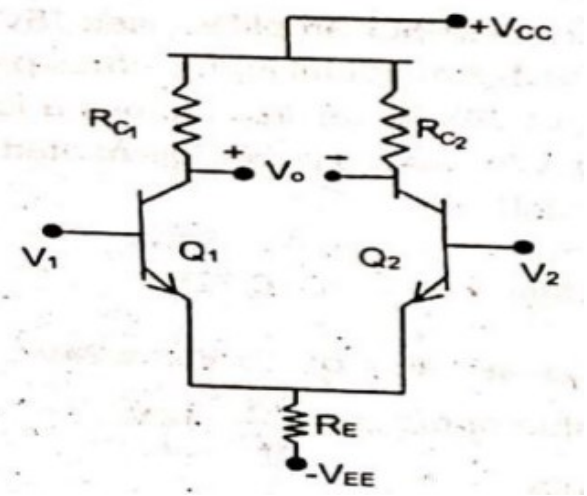
Comparison of all configurations : (h-parameter model)

SNO	Configuration	A_d	R_i	R_o
1	Dual Input balanced output	$\frac{-hfe\ Rc}{(Rs + hie)}$	$2(R_s + hie)$	R_C
2	Dual input unbalanced output	$\frac{-hfe\ Rc}{2(Rs + hie)}$	$2(R_s + hie)$	R_C
3	Single input Balanced output	$\frac{-hfe\ Rc}{(Rs + hie)}$	$2(R_s + hie)$	R_C
4	Single input unbalanced output	$\frac{-hfe\ Rc}{2(Rs + hie)}$	$2(R_s + hie)$	R_C

A differential amplifier is shown below, has following specifications.

$R_{C_1} = R_{C_2} = 1.8K\Omega, R_E = 4K\Omega, V_{CC} = 10V, -V_{EE} = -10V$

$\beta = 100$ and $V_{BE} = 0.7\ V$



The emitter current I_E is

(A) 2.3mA (B) 1.16mA

(C) 1.7mA (D) 0.98mA

Sol. $2I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{10 - 0.7}{4K}$

$\Rightarrow I_E = \dfrac{9.3}{8}\text{mA} = 1.16\text{mA}.$ Choice (B)

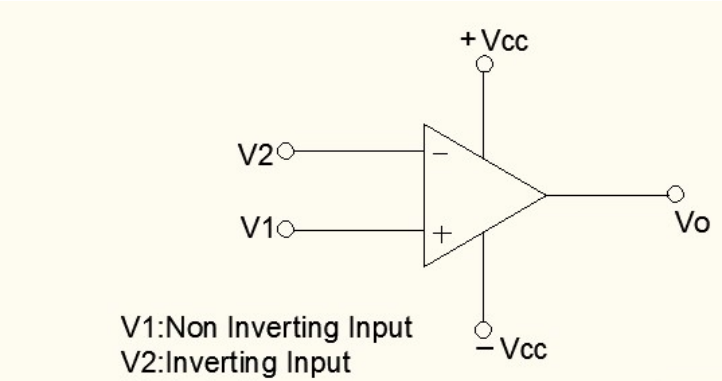
OPERATIONAL AMPLIFERS (IC741)

Operational Amplifier, also called as an Op-Amp, is a basic integrated circuit, which can be used to perform various linear, non-linear, and mathematical operations. linear applications like voltage follower, differential amplifier, inverting amplifier, non-inverting amplifier, etc. and non-linear applications like precision rectifiers, comparators, clampers, Schmitt trigger circuit, etc. it is designed to perform mathematics operations like addition, subtraction, differentiation, integration, multiplication, division etc.,

An op-amp is a direct coupled high gain negative feedback amplifier. *It can amplify the signals in the range of 0Hz to 1MHz. It is a basic linear integrated circuit.* You can operate op-amp both with AC and DC signals.

IC741 operational amplifier is an 8bit dual in line package IC. It is a very popular type IC. It has ***five basic terminals.***

- Two input terminals
- One output terminal
- Two supply terminals

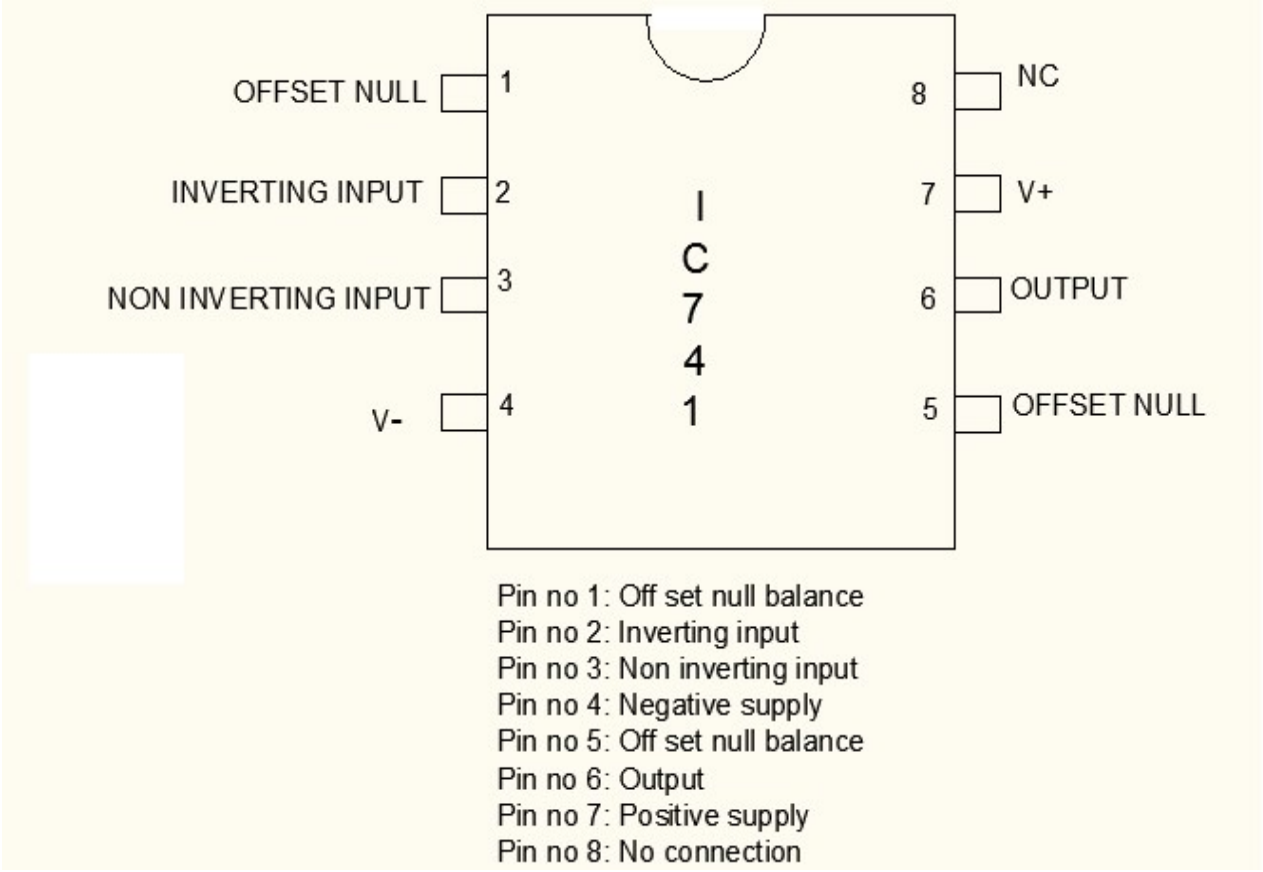


An op-amp consists of differential amplifier(s), a level translator and an output stage. A differential amplifier is present at the input stage of an op-amp and hence an op-amp consists of **two input terminals.**

One of those terminals is called as the inverting terminal and the other one is called as the non-inverting terminal. The terminals are named based on the phase relationship between their respective inputs and outputs.

The signal given to the inverting input in always inverted at its output. A positive voltage at the inverting input produces a negative output voltage, and similarly a negative input voltage produces a positive output voltage. But the signal given to the non-inverting input will not produce any sign change at the output. The functions of an op-amp generally depends upon the external connected components.

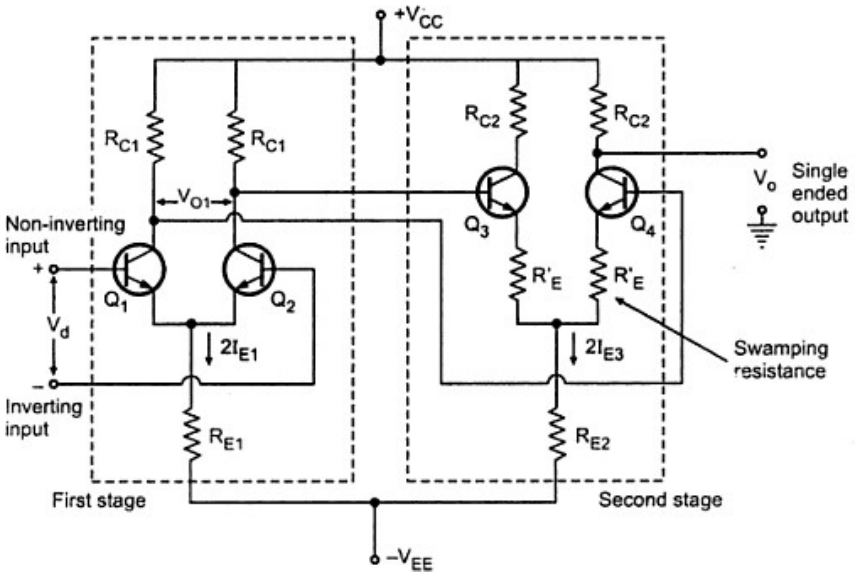
PIN DIAGRAM OF OP-AMP IC 741



Pin no 1: Off set null balance
Pin no 2: Inverting input
Pin no 3: Non inverting input
Pin no 4: Negative supply
Pin no 5: Off set null balance
Pin no 6: Output
Pin no 7: Positive supply
Pin no 8: No connection

Cascade Differential Amplifier Stages

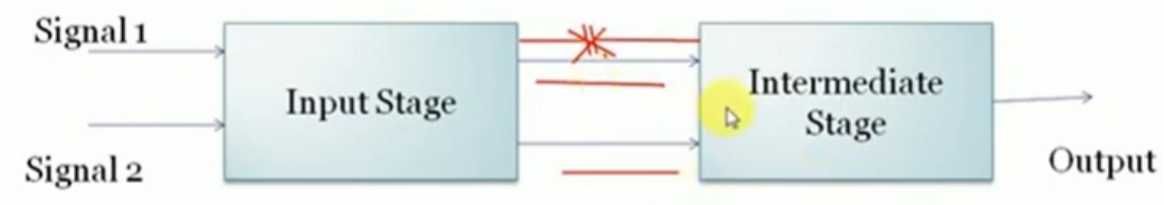
In cascaded differential amplifier, the output of the first stage is used as an input for the second stage, the output of the second stage is applied as an input to the third stage, and so on. Because of direct coupling between the stages, the operating point of succeeding stages changes Level Translator:



Because of the direct coupling the dc level at the emitter rises from stages to stage. This increase in dc level tends to shift the operating point of the succeeding stages and therefore limits the output voltage swing and may even distort the output signal.

To shift the output dc level to zero, level translator circuits are used. An emitter follower with voltage divider is the simplest form of level translator as shown in fig Thus a dc voltage at the base of Q produces 0V dc at the output. It is decided by R1 and R2. Instead of voltage divider emitter follower either with diode current bias or current mirror bias as shown in fig may be used to get better results.

level shifter or translator:

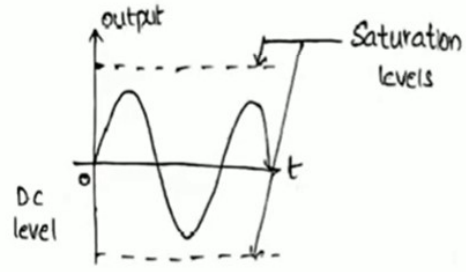


❖ As the coupling capacitors are not used to couple the amplifiers in the intermediate stage, the dc biasing voltage level propagates through the amplifier chain.

❖ So, at the final output, along with AC signal, DC component/signal will present.

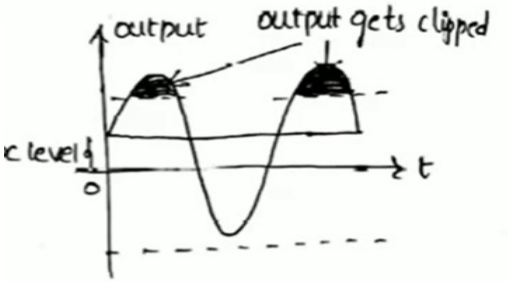
❖The effects due to the presence of DC component are:

- The output gets distorted (since operating point changes)
- It limits the maximum output voltage swing.



Output with zero DC level

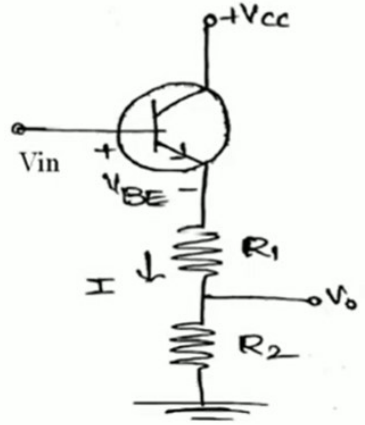
❖ The main purpose of level shifting stage is to shift the output quiescent d.c level towards the ground with minimum change in a.c signal.



Distorted output due to the presence of DC level

level shifter or translator:

Emitter follower with voltage divider circuit



Apply KVL to the Base-Emitter loop,

$$-V_i + V_{BE} + IR_1 + IR_2 = 0$$

$$I = \frac{V_i - V_{BE}}{R_1 + R_2}$$

$$V_o = IR_2$$

Substitute the value of I in Vo, we get

$$\therefore V_o = \left(\frac{V_i - V_{BE}}{R_1 + R_2}\right) * R_2$$

- By proper selection of R1 and R2, the DC level in output voltage, Vo will be controlled.
- The main drawbacks are:
  1. The output impedance is high.
  2. The signal voltage gets attenuated by the factor (R2/(R1+R2))

level shifter or translator: **Emitter follower with current mirror**

In current mirror input current is equal to output current

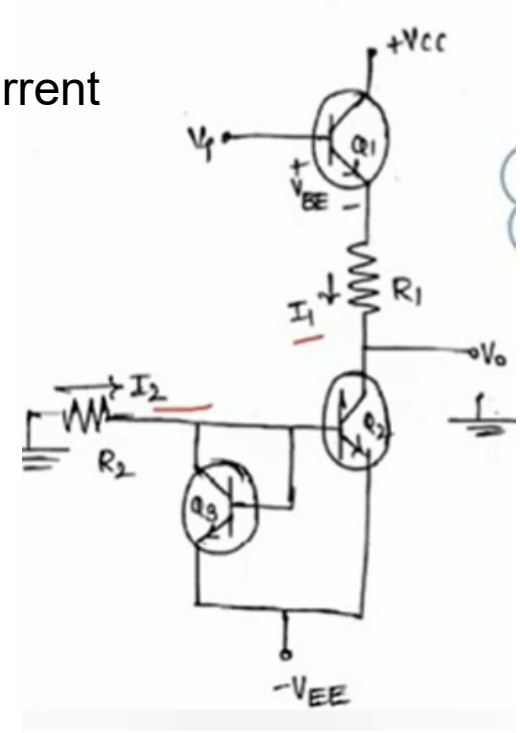
$$I_1 = I_2$$

$$I_2 = I_1 = \frac{V_{EE} - V_{BE}}{R_1}$$

Apply KVL to the Base-Emitter loop of Q1,

$$-V_1 + V_{BE} + I_1 R_1 + V_o = 0$$

$$V_o = V_1 - V_{BE} - I_1 R_1$$



Specifications

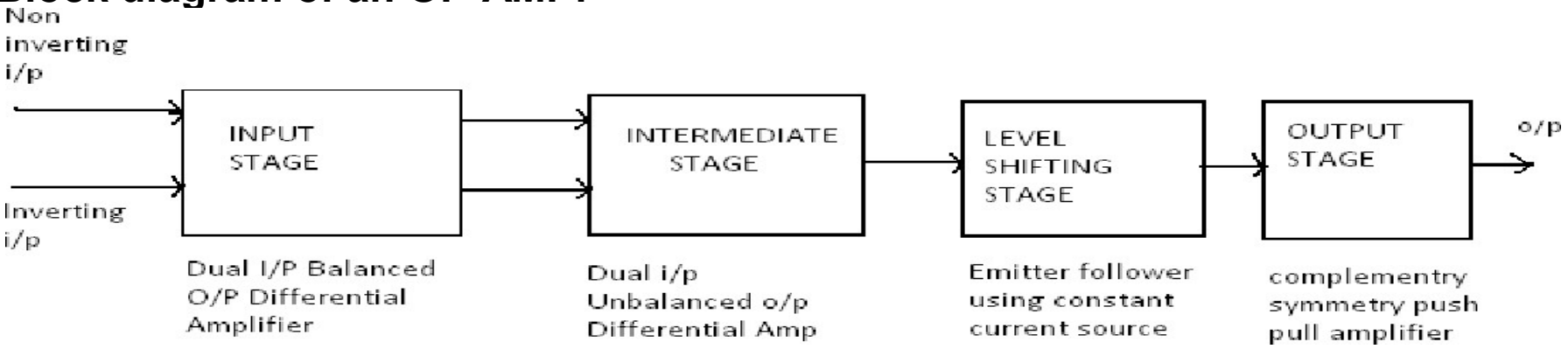
2.6 FET OPERATIONAL AMPLIFIER

The op-amp circuits discussed so far are bipolar op-amps. Op-amps using field transistors (FETs) in the input stage offer some very significant advantages over bipolar op-amps, especially in areas as input impedance, input bias and offset currents and slewing rate as shown in Table 2.1.

Table 2.1

Parameter	BJT	JFET	MOSFET
Input resistance	kΩ	10^9 Ω (giga-ohms)	10^{12} Ω (tera-ohms)
Input gate current	μA	1 nA	1 pA
Input offset current	20 nA	2 pA	0.5 pA
Slewing rate	1 V/μs	3 V/μs	10 V/μs

Block diagram of an OP-AMP:



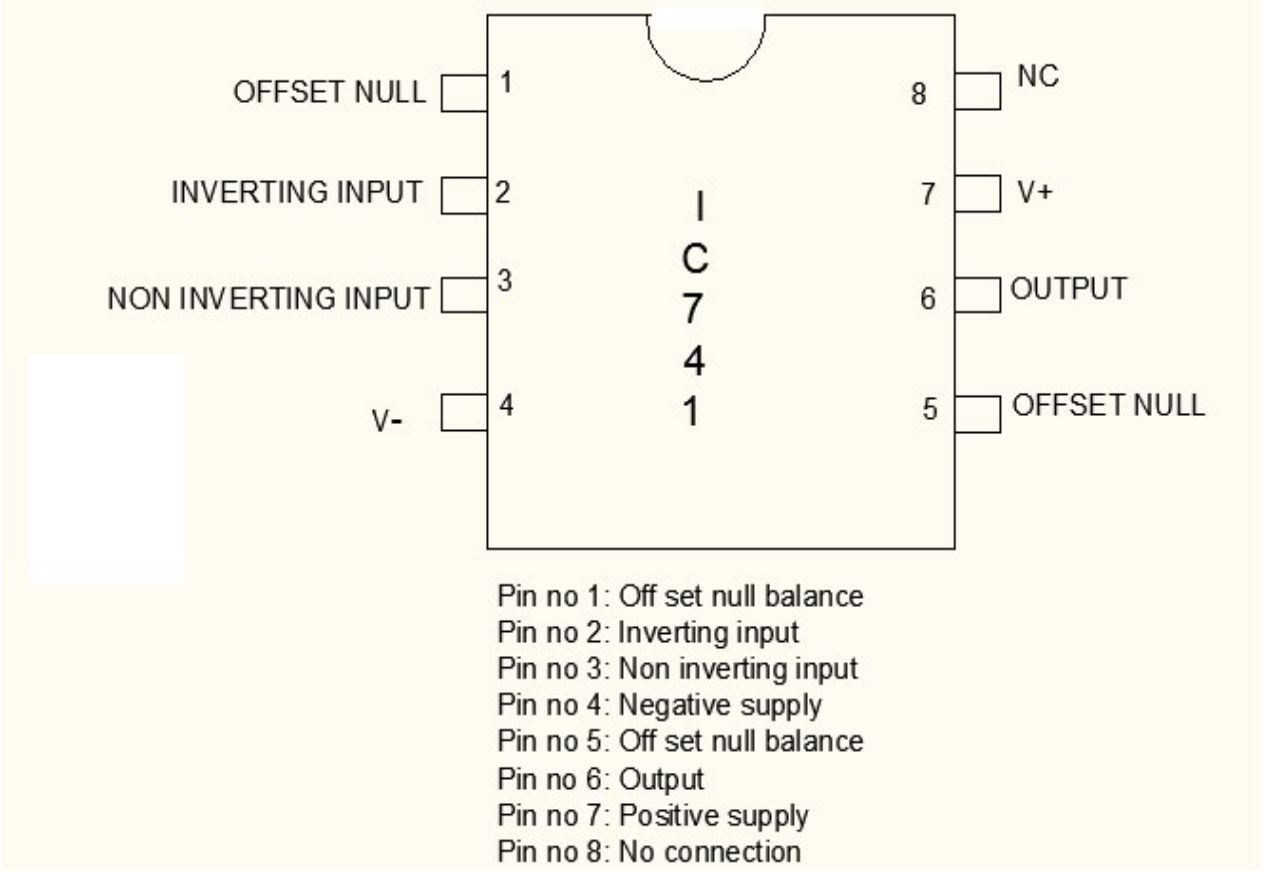
The internal block diagram of an op-amp is shown in the fig The input stage is the dual input balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp.

The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. On most amplifiers, the intermediate stage is dual input, unbalanced output. Because of direct coupling, the dc voltage at the output of the intermediate stage is well above ground potential.

Therefore, the level translator (shifting) circuit is used after the intermediate to prevent undesired dc current in the load and increasing the permissible output voltage swing. Finally, it produces large output voltage or current.

The final stage is usually a push pull complementary symmetry amplifier output stage. The output stage increases the voltage swing and raises the ground supplying capabilities of the op-amp. A well designed output stage also provides low output resistance.

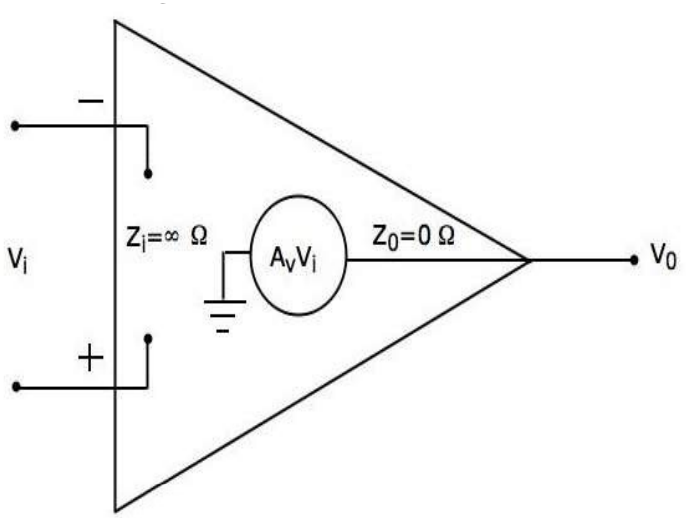
PIN DIAGRAM OF OP-AMP IC 741



Pin no 1: Off set null balance
Pin no 2: Inverting input
Pin no 3: Non inverting input
Pin no 4: Negative supply
Pin no 5: Off set null balance
Pin no 6: Output
Pin no 7: Positive supply
Pin no 8: No connection

IDEAL OP-AMP:

An ideal op-amp exists only in theory, and does not exist practically. The **equivalent circuit of an ideal op-amp is show**

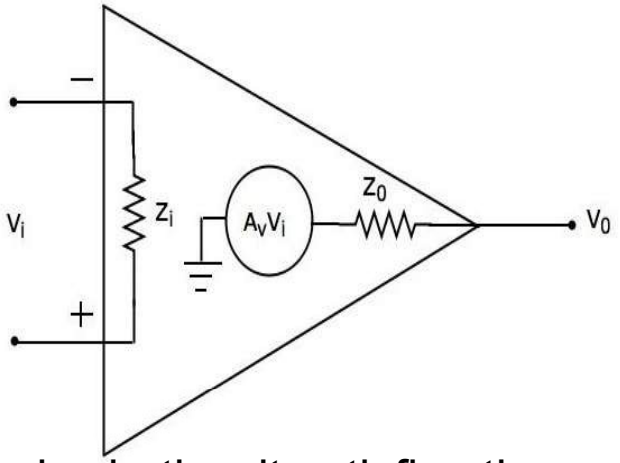


An **ideal op-amp exhibits the following characteristics:**

- Input impedance $\boldsymbol{Zi} = \infty\ \boldsymbol{\Omega}$
- Output impedance $\boldsymbol{Z0} = \boldsymbol{0}\ \boldsymbol{\Omega}$
- Open loop voltage gain $\boldsymbol{Av} = \infty$
- If (the differential) input voltage $\boldsymbol{Vi} = \boldsymbol{0}\ \boldsymbol{V}$, then the output voltage will be $\boldsymbol{V_0} = \boldsymbol{0}\ \boldsymbol{V}$
- Bandwidth is **infinity. It means, an ideal op-amp will amplify the signals of any** frequency without any attenuation.
- Common Mode Rejection Ratio (**CMRR) is infinity.**
- Slew Rate (**SR) is infinity. It means, the ideal op-amp will produce a change in** the output instantly in response to an input step voltage.

Practical Op-Amp

Practically, op-amps are not ideal and deviate from their ideal characteristics because of some imperfections during manufacturing. The **equivalent circuit of a practical op-amp** is shown in the following figure:



A **practical op-amp exhibits the following characteristics:**

- Input impedance, Zi in the order of **Mega ohms.**
- Output impedance, $Z0$ in the order of **few ohms.**
- Open loop voltage gain, Av will be **high.**

When you choose a practical op-amp, you should check whether it satisfies the following conditions:

- Input impedance, Zi should be as high as possible.
- Output impedance, $Z0$ should be as low as possible.
- Open loop voltage gain, Av should be as high as possible.
- Output offset voltage should be as low as possible.
- The operating Bandwidth should be as high as possible.
- CMRR should be as high as possible.
- Slew rate should be as high as possible.

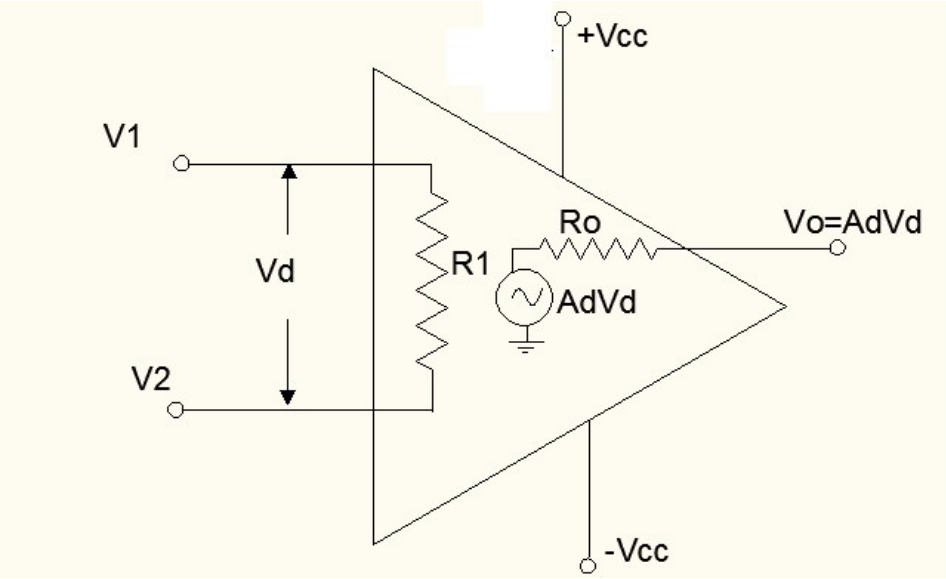
Note: IC 741 op-amp is the most popular and practical op-amp.

Application of op-amp

- Audio and video pre-amplifiers and buffers
- Voltage comparators
- Differential amplifiers
- Differentiators and integrators
- Filters
- Precision rectifiers
- Precision Peak Detector
- Voltage and current regulators
- Analogue calculators
- Voltage clamp
- Analog-to-digital converters
- Digital-to-analog converters

Ideal Characteristics of op-amp:

Characteristics Parameter	Ideal value	Practical value
Voltage Gain (Av)	∞	≈ 10^6
Input Resistance (Ri)	∞	≈ 1 MΩ
Output Resistance (R0)	0	≈ 10 Ω to 100 Ω
Bandwidth (B.W)	∞	≈ 1 MHz
Slew Rate (S.R)	∞	≈ 80 V/μs



The figure represents equivalent circuit of op-amp.

In general the output voltage of an op-amp **V0 = Ad Vd = Ad (V2-V1)**

Ad = large signal open loop voltage gain
Vd = differential input voltage
V1 = inverting input voltage with respect to ground
V2 = non- inverting input voltage with respect to ground

PARAMETERS OF OP-AMP:

Input offset voltage: It is the input voltage which should be applied between the input terminals to get zero output voltage.

Input offset current: It is the difference between the currents entering the inverting and non-inverting input terminals of an operational amplifier.

Input bias current: It is the average of the currents that enter into the inverting and non-inverting input terminals of a operational amplifier.

Output offset voltage: It is the output voltage present, when the two input terminals are grounded.

Differential input resistance: It is the equivalent resistance that can be calculated at either the inverting or non-inverting input terminal with the other terminal connected to ground.

Input capacitance: It is the equivalent capacitance that can be calculated at either the inverting or non-inverting terminal with the other terminal connected to ground.

Open loop voltage gain (Av): When the op-amp is used without any feedback, the differential voltage gain is known as open loop voltage gain.

Supply voltage rejection ratio (SVRR): It occurs because of supply voltage variations, which leads to changes in input offset voltage.
SVRR is the ratio of the change in input offset voltage to the corresponding change in one power supply voltage, with all remaining power voltages held constant.

Output voltage swing: It is the maximum peak-to-peak output voltage (+ve or – ve saturation voltage) which can be obtained without waveform clipping when DC output is zero.

Slew rate (SR): It is defined as the maximum rate of change of output voltage per unit of time. It is expressed in volts per microseconds.

$$\mathbf{SR} = (\mathbf{dV0/dt})_{\mathbf{maximum}}$$

Common mode rejection ratio (CMRR): CMRR is the ratio of differential voltage gain (A_d) to the common mode voltage gain (A_{cm}).

$$\mathbf{CMRR} = \mathbf{A_d/A_{cm}}$$

Maximum differential input voltage: It is the maximum value of differential input voltage that can be applied without damaging the op-amp.

Maximum common mode input voltage: It is the maximum voltage to which that the two inputs can be raised above ground potential before the op-amp.

An ideal op-amp exhibits the following characteristics:

- Input impedance $\boldsymbol{Zi} = \infty\boldsymbol{\Omega}$
- Output impedance $\boldsymbol{Z0} = \mathbf{0}\ \boldsymbol{\Omega}$
- Open loop voltage gain $\boldsymbol{Av} = \infty$
- If (the differential) input voltage $\boldsymbol{Vi} = \mathbf{0}\ \boldsymbol{V}$, then the output voltage will be $\boldsymbol{V0} = \mathbf{0}\ \boldsymbol{V}$
- Bandwidth is infinity. It means, an ideal op-amp will amplify the signals of any frequency without any attenuation.
- Common Mode Rejection Ratio (CMRR) is infinity.
- Slew Rate (SR) is infinity. It means, the ideal op-amp will produce a change in the output instantly in response to an input step voltage.

A practical op-amp exhibits the following characteristics:

- Input impedance, $\boldsymbol{Zi}$ in the order of Megaohms.
- Output impedance, $\boldsymbol{Z0}$ in the order of few ohms.
- Open loop voltage gain, $\boldsymbol{Av}$will be high.

When you choose a practical op-amp, you should check whether it satisfies the following conditions:

- Input impedance, $\boldsymbol{Zi}$ should be as high as possible.
- Output impedance, $\boldsymbol{Z0}$ should be as low as possible.
- Open loop voltage gain, $\boldsymbol{Av}$ should be as high as possible.
- Output offset voltage should be as low as possible.
- The operating Bandwidth should be as high as possible.
- CMRR should be as high as possible.
- Slew rate should be as high as possible.

DC CHARACTERISTICS OF OP-AMP:

If there is no input a.c. Signal, the output should be zero but practically some output is present(error in output) due to parameter such as Input bias current, Input offset current, Input offset voltage, Thermal drift and output offset voltage.
To overcome this and get Zero output if input is zero, compensate above parameters.

An ideal op amp draws no current from the source and its response is also independent of temperature.

But practical op amp does not work this way. Current is taken from the source into the op amp inputs. Also the two inputs responds differently to current and voltages due to mismatch in transistors.

Practical op amp shifts its operation with temperature.

These non ideal dc characteristics that add error to the DC output voltage.

The DC characteristics are

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

INPUT BIAS CURRENT

The op-amp's input is made up of differential amplifier, which can be made of BJT or FET. In an ideal op-amp, we assumed that no current is drawn from the input terminals due to infinite impedance of op-amp. However practical op amp, the base currents entering into the inverting and non-inverting terminals (IB- & IB+ respectively). Even though both the transistors are identical, IB- and IB+ are not exactly equal due to internal imbalance between the two inputs. Input bias current and Inverting amplifier with bias currents is shown in figure

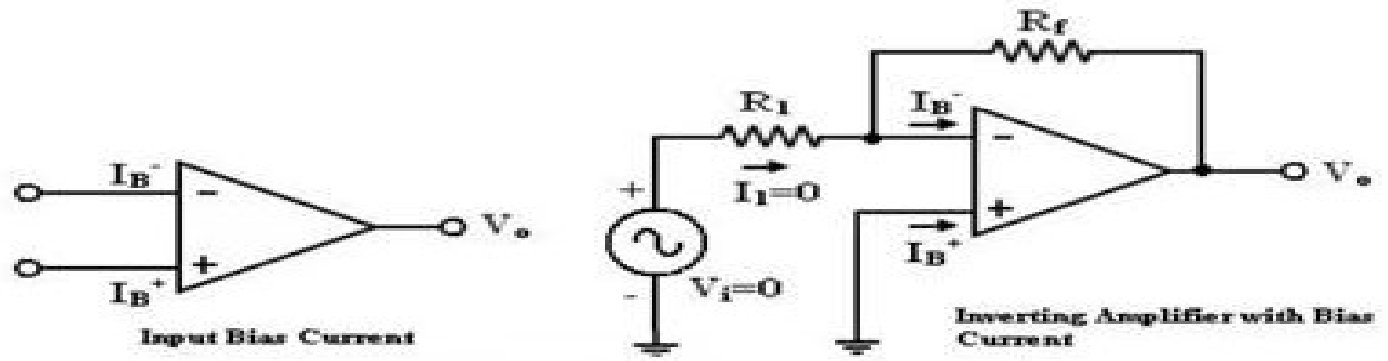


Figure a) input bias current b) Inverting amplifier with bias currents

input bias current is average of base currents entering into non iverting and inverting terminals

input bias current $I_B = \dfrac{I_B^+ + I_B^-}{2}$

If input voltage Vi = 0V. The output Voltage Vo should also be (Vo = 0) zero, but for IB = 80nA (typical value of op-amp) We find that the output voltage is offset by Op-amp with a 1M feedback resistor

$$Vo = IB^{-} \times R_f = 80nA \times 1M = 80mV$$

The output is driven to 80mV with zero input, because of the bias currents.

In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated by a compensation resistor R_{comp} has been added between the non-inverting input terminal and ground as shown in the figure

Current IB+ flowing through the compensating resistor Rcomp, then by KVL we get,

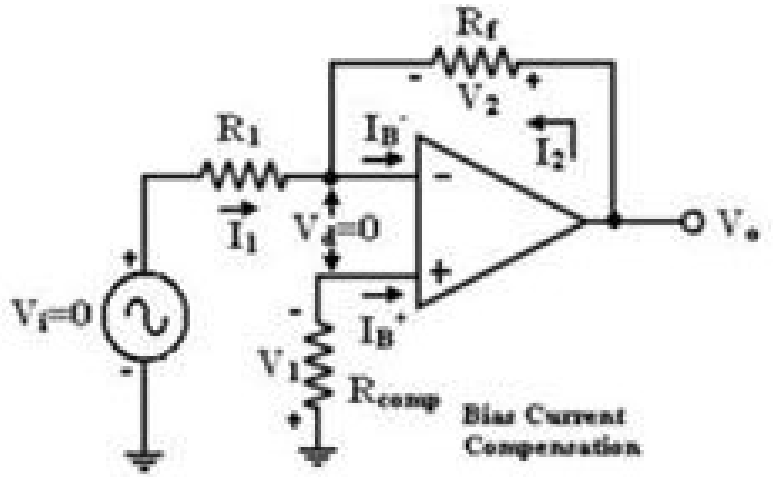
$$- V1+0+V2-Vo = 0 \text{ (or)}$$

$$Vo = V2 - V1 \text{ -------- (1)}$$

By selecting proper value of Rcomp, V2 can be cancelled with V1 and the Vo = 0. The value of Rcomp is derived as

$$V1 = IB^{+} \times R_{comp} \text{ (or)}$$

$$IB+ = V1/Rcomp \text{ ---------- (2)}$$



Bias compensated circuit in non-inverting amplifier

The node '' is at voltage ($-V_1$). Because the voltage at the non-inverting input terminal is ($-V_1$).
So with $V_i = 0$ we get,

$$I1 = V1/R1 \text{ ---------- (3)}$$

$$I2 = V2/Rf \text{ ---------- (4)}$$

For compensation, Vo should equal to zero (Vo = 0, Vi = 0). i.e. from equation (3) V2 = V1. So that,

$$I2 = V1/Rf \text{ ——> (5)}$$

KCL at node 'b' gives,

$$IB^- = I_2 + I_1 = (V_1/R_f) + (V_1/R_1) = V_1(R_1+R_f)/R_1R_f \text{ ---------- (5)}$$

Assume $IB^- = IB^+$ and using equation (2) & (5) we get

$$V_1 (R_1+R_f)/R_1R_f = V_1/R_{comp}$$

$$R_{comp} = R_1 \parallel R_f \text{ ---------- (6)}$$

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

INPUT OFFSET CURRENT:

It is the difference between the currents entering the inverting and non-inverting input terminals of an operational amplifier.

i. Bias current compensation will work if both bias currents IB+ and IB- are equal.
ii. Since the input transistors cannot be made identical. There will always be some small difference between IB+ and IB-. This difference is called the offset current

$$|I_{os}| = I_{B+} - I_{B-} \text{ ---------- (7)}$$

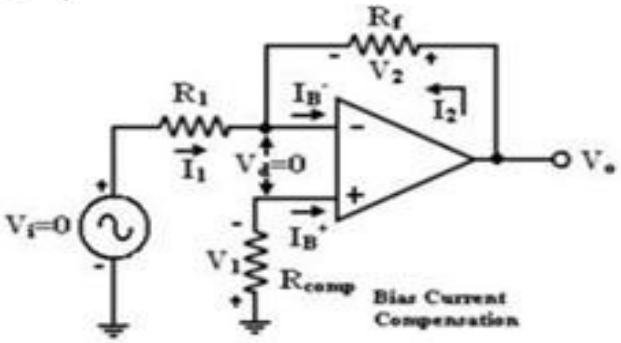
Offset current Ios for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when Vi = 0.

$$V_1 = I_B^+ R_{comp} \text{ ---------- (11)}$$

$$\text{And } I_1 = V_1/R_1 \text{ ---------- (12)}$$

KCL at node a gives,

$$I_2 = (I_B^- - I_1) = I_B^- - (I_B^+ \frac{R_{comp}}{R_1})$$



Output voltage $Vo = R_f I_{OS}$

Again $V_0 = I_2 R_f - V_1$

Vo = I2 Rf - IB+ Rcomp

Vo = 1M Ω X 200nA

Vo = 200mV with Vi = 0

By using the above Equation the offset current can be minimized by keeping feedback resistance small.

- Unfortunately to obtain high input impedance, R1 must be kept large.
- R1 large, the feedback resistor R_f must also be high. So as to obtain reasonable gain.

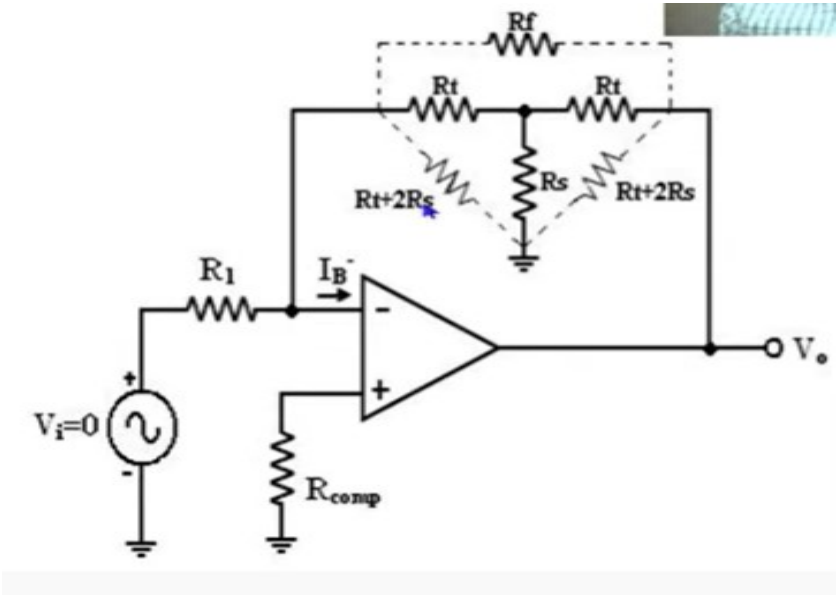
The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

The T-network provides a feedback signal as if the network were a single feedback resistor.

- T feedback network can be calculated as:

$$R_t << \frac{R_f}{2}$$

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$



INPUT OFFSET VOLTAGE

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [Vo ≠ 0 with Vi= 0]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the either input terminal to make output (Vo) = 0. figure 1.6.3 a) shown below is the op-amp showing input offset voltage. This voltage is called input offset voltage Vos. This is the voltage required to be applied at the input for making output voltage to zero (Vo = 0).

The differential voltage must be applied between two the two terminals of op-amp, to make output voltage is zero. It is denoted as input offset voltage Vos.

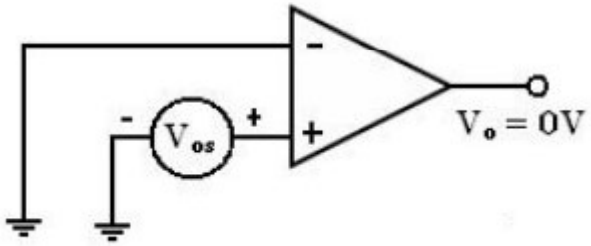


Figure 1.6.3 a)op-amp showing input offset voltage

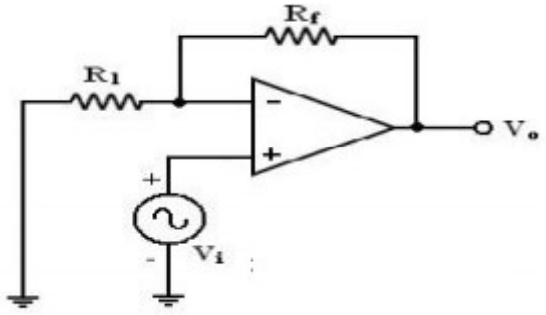
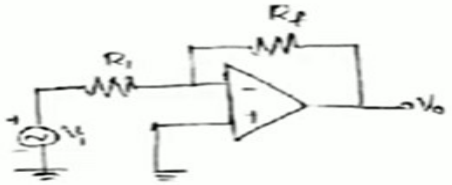
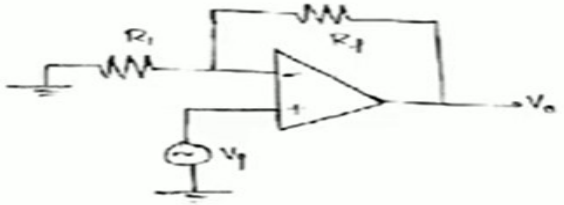


Figure 1.6.3 b)Non-inverting Amplifier

❖Let us consider, the inverting and non-inverting Op-Amp of closed loop is shown as,



Inverting Amplifier



Non-Inverting Amplifier

- Assume $V_i = 0$
- $V_{ios} = |V_i - V_2|$
- $V_{ios} = |0 - V_2|$
- $V_{ios} = V_2$

$$V_2 = \frac{R_1}{R_1 + R_f} V_0$$

$$V_0 = \frac{R_1 + R_f}{R_1} V_2 = \left[1 + \frac{R_f}{R_1}\right] V_2$$

$$V_0 = \left[1 + \frac{R_f}{R_1}\right] V_{ios}$$

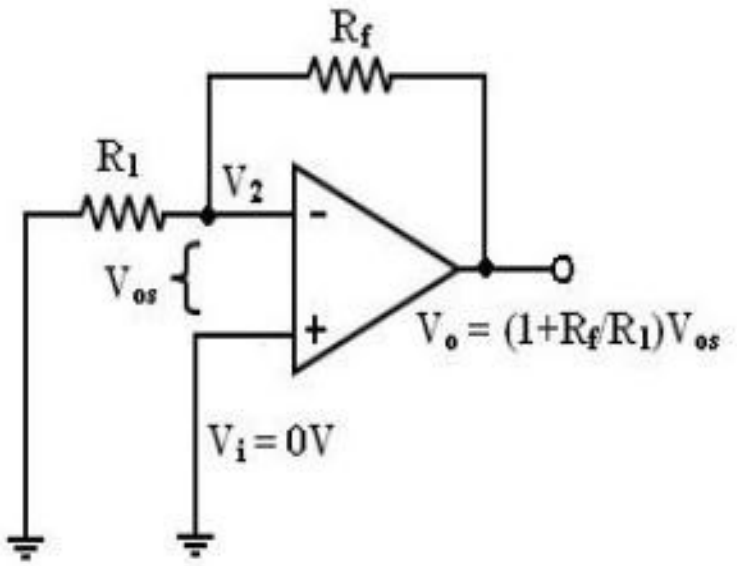


Figure 3c) Inverting Amplifier

Minimal amount of V_{ios}, we can obtain output V_0 is zero. This is one of the parameter to effecting the output voltage is zero if input is zero.

TOTAL OUTPUT OFFSET VOLTAGE

The total output offset voltage VOT could be either more or less than the offset voltage produced at the output due to input bias current (IB) or input offset voltage alone(Vos). This is because IB and Vos could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure 1.6.3 b, c) without any compensation technique used is given by many op amps provide offset compensation pins to nullify the offset voltage.

A 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4. The position of the wipes is adjusted to nullify the offset voltage. Compensation circuit for offset voltage is shown in figure 1.6.4.

When the given (below) op-amps does not have these offset null pins, external balancing techniques are used.

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_B$$

With Rcomp, the total output offset

$$V_{OT} = \left(1 + \frac{R_f}{R_1}\right) V_{OS} + R_f I_{OS}$$

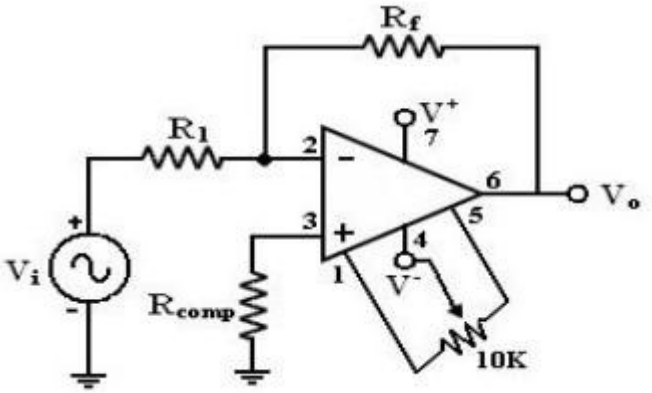


Figure 1.6.4. compensation circuit for offset voltage

THERMAL DRIFT

Bias current, offset current, and offset voltage change with temperature. A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift. Offset current drift is expressed in nA/ºC. These indicate the change in offset for each degree Celsius change in temperature.

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

ΔV_{ios} = Change in input offset voltage

ΔT = Change in temperature

$$\text{Thermal drift in input bias current} = \frac{\Delta I_b}{\Delta T}$$

$$\text{Thermal drift in input offset current} = \frac{\Delta I_{ios}}{\Delta T}$$

AC Characteristics: For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

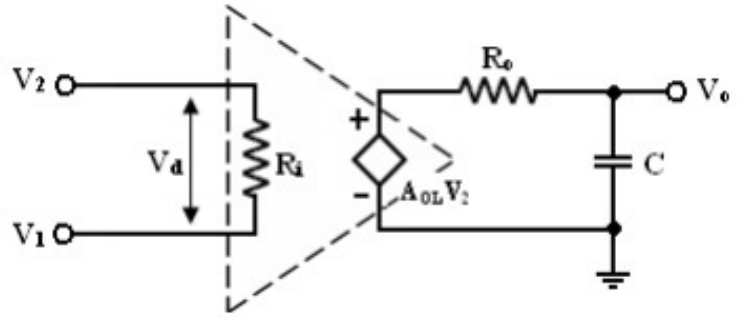
Frequency Response:

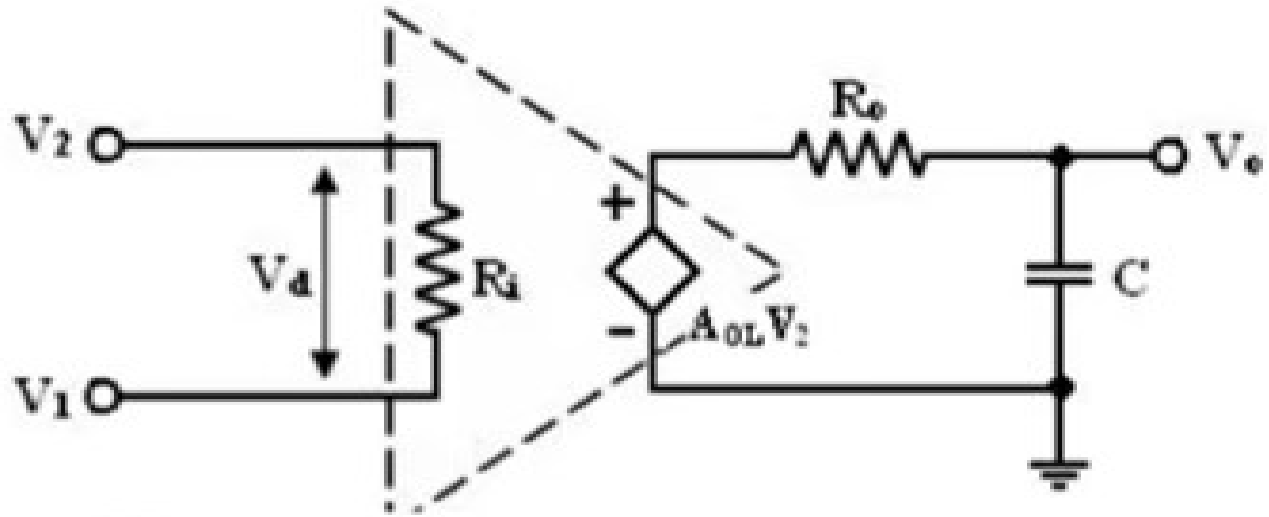
The variation in operating frequency will cause variations in gain and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response.

Op-amp should have an infinite bandwidth Bw =∞ (i.e) if its open loop gain should constant with dc signal, a.c. signal and up to high radio frequency.

For practical the op-amp gain decreases (roll-off) at higher frequency. The op-amp gain decreases at higher frequency there must be a capacitive component present at output of circuit of the op-amp . For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C shown in below fig. This fig. represents high frequency model of op-amp with single corner frequency. fig is a modified variation of the low frequency model with capacitor C at the o/p. **The op-amp gain decreases at high frequencies due to junction capacitance present at output of op-amp.**

There is one pole due to R_0C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from the fig. Capacitance will get added to output of op amp.





$$v_o = \frac{-jX_c}{R_o - jX_c} A_{OL} v_d$$

$$A = \frac{v_o}{v_d} = \frac{A_{OL}}{1 + j\,2\pi f R_o C}$$

$$A = \frac{A_{OL}}{1 + j(f/f_1)}$$

$$f_1 = \frac{1}{2\pi R_o C}$$

$$|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}$$

$$\phi = -\tan^{-1}(f/f1)$$

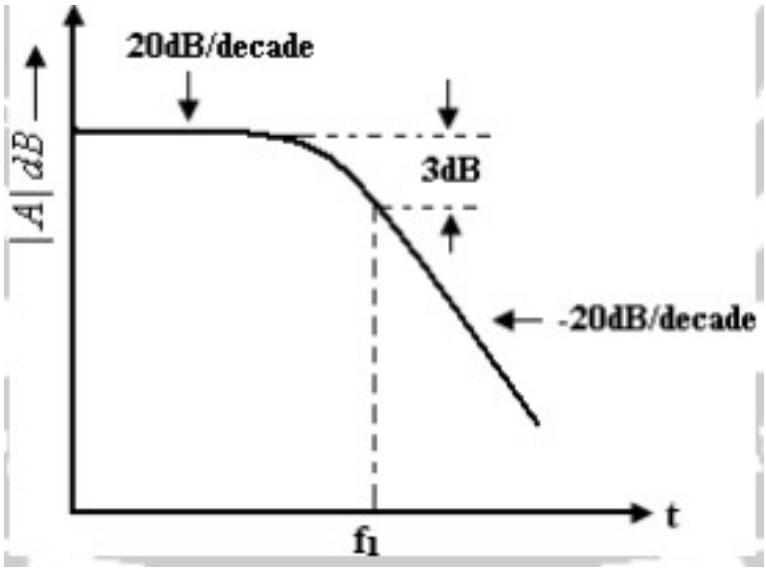
phase, $\phi = \tan^{-1}\left(\frac{0}{A_{OL}}\right) - \tan^{-1}\left((f/f_c)(1)\right)$

$\phi = -\tan^{-1}(f/f_c)$

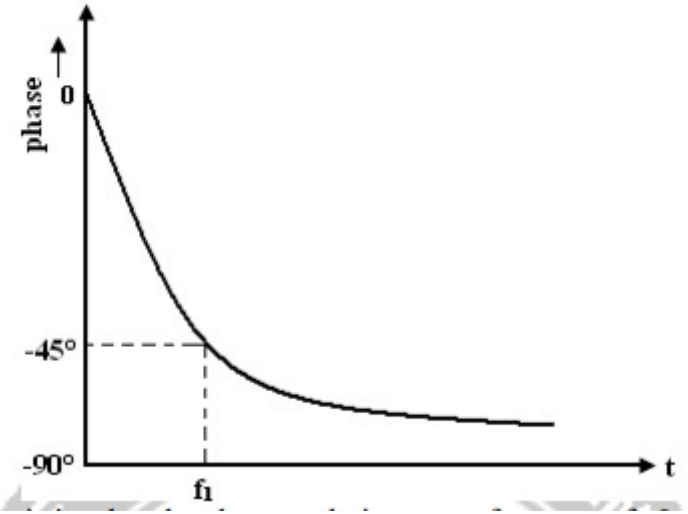
f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as,

The magnitude and phase angle characteristics

1. For frequency f<< f1 the magnitude of the gain is 20 log AOL in dB.
2. At frequency f = f1 the gain in 3 dB down from the maximum value of AOL in dB. This frequency f1 is called corner frequency.
3. For f>> f1 the gain roll-off at the rate off -20dB/decade or-6dB/decade.



Gain vs frequency characteristics



Phase characteristics

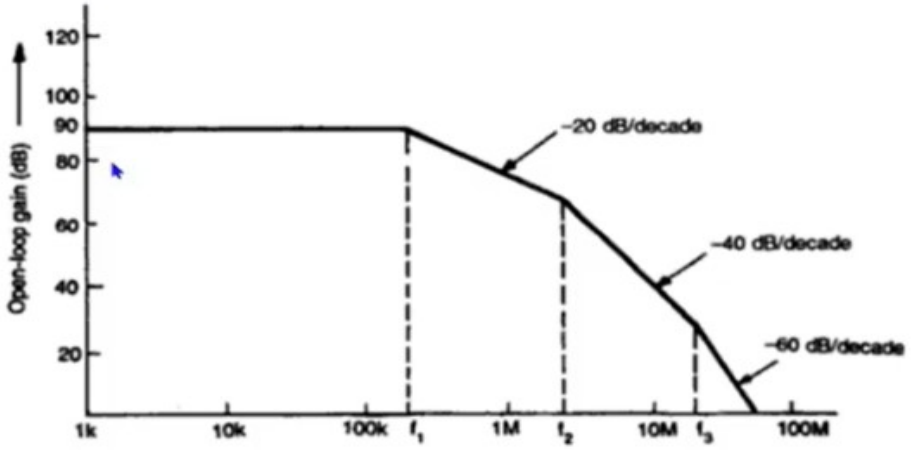
If the op-amp operates with more than One corner frequencies

$$A = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}; 0 < f_1 < f_2 < f_3$$

Gain in S- domain

$$A = \frac{A_{OL} \cdot \omega_1 \cdot \omega_2 \cdot \omega_3}{(s + \omega_1)(s + \omega_2)(s + \omega_3)}$$

Where ω is angular frequency



From the fig. Gain at lower frequency is maximum, the gain started decrement at first corner frequency, the frequency at first corner frequency gain is decreased by -20db/decade, second corner frequency gain roll of by -40dB/decade, and third corner frequency is decreased by -60dB/decade.

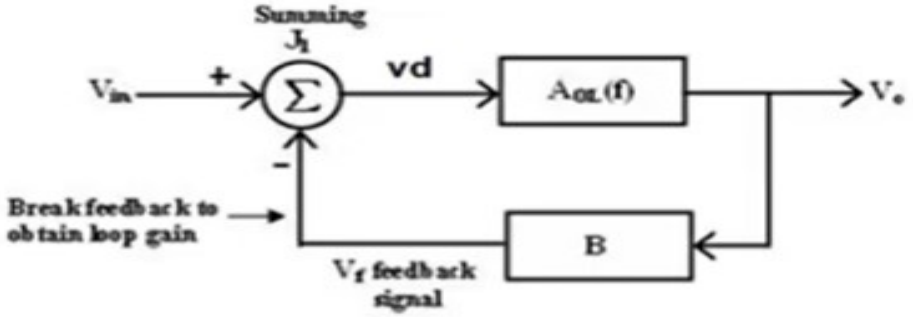
- Open loop gain verses frequency

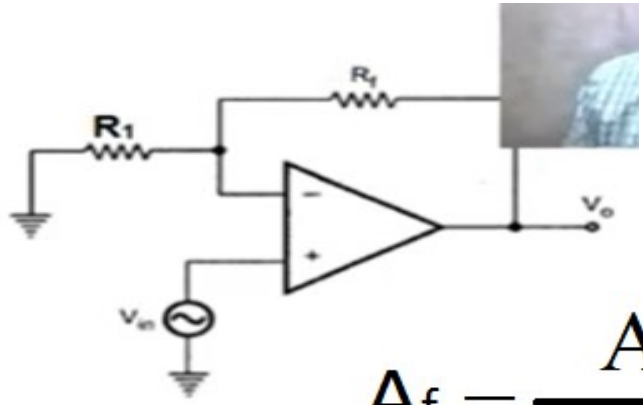
Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable system keeps on increasing until the system break down. The unstable system are impractical and need be made stable. The criterian for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.

Circuit stability:

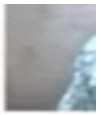
- Op-amps are rarely used in the open loop configuration.
- Due to its use in closed loop configuration, it is necessary to study the effect of feedback on the circuit stability.
- Consider a Non inverting amplifier with resistive feedback.



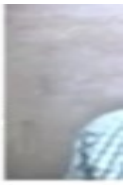


$$A_f = \frac{A}{1+A\beta}$$

- Forward block & feedback block.
- As the feedback block uses only resistive elements and hence its transfer function B is independent of frequency.

- Stability of the circuit is depends on the behavi  of the roots of the characteristic equation. $1+A_{OL}$. $B = 0$
- Determining stability of circuit means, deciding how close the circuit is to the conditions of sustained oscillations.
- The system is said to be stable if its output reaches a fixed value within a finite time.
- The critical values of loop gain are 0dB and -180^{o}
- **Gain Margin(G.M) :**
- $$G.M = -20 \log | A_{OL}(f)\, \beta | \ dB$$
- **Phase Margin (P.M)**
- $$P.M = 180^{o} + \angle A_{OL}(f)\, \beta$$
- If G.M is positive (i.e., $A_{OL}(f)\, \beta$ is –ve) then the system is stable.
- The negative values of GM & PM indicate instability of the system.

Frequency compensation:



- The op-amp circuit with single break or corner frequ is inherently stable.
- Frequency compensation technique is used
  - — To get larger band width with lower closed loop gain
  - — To alter the response as per the requirement.
- There are 2 compensation techniques.
  1) External compensation
  2) Internal compensation

Frequency compensation:

1) external frequency compensation:

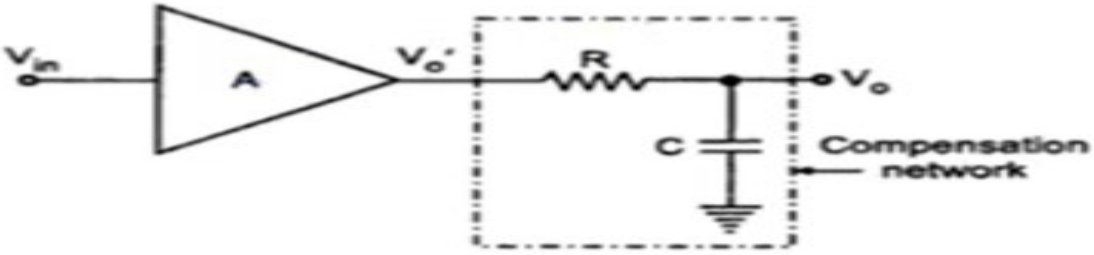
There are 2methods:

1. Dominant pole
2. Pole-zero compensation

Dominant pole compensation:

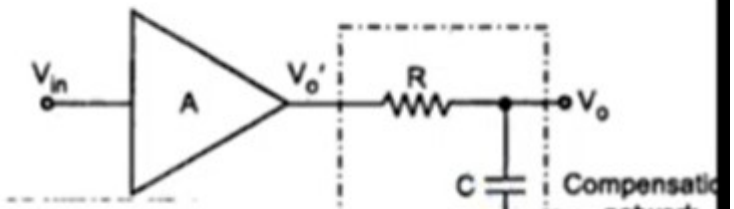
- Consider an op-amp with three break frequencies and with loop gain is A.

$$A = \frac{A_{OL}}{(1+j\frac{f}{f_1})(1+j\frac{f}{f_2})(1+j\frac{f}{f_3})}$$



- Dominant pole is introduced by adding a compensating network (R-C Network).
- The dominant pole means the pole with magnitude much smaller than the existing poles.
- The break frequency of the compensating network is the smallest compared to the existing break frequencies.

- The transfer function of the compensating network can be obtained as:



A_1 = Transfer function of compensating network

$$= \frac{V_o}{V_o'}$$

By the voltage divider rule applied to the network,

$$A_1 = \frac{V_o}{V_o'} = \frac{-jX_C}{R - jX_C}$$

$$A_1 = \frac{1}{1 + j\left(\frac{f}{f_d}\right)}$$

$$A' = AA_1$$

Hence, the compensated transfer function becomes

$$A' = \frac{A_{OL}}{(1 + j\frac{f}{f_d})(1 + j\frac{f}{f_1})(1 + j\frac{f}{f_2})(1 + j\frac{f}{f_3})}$$

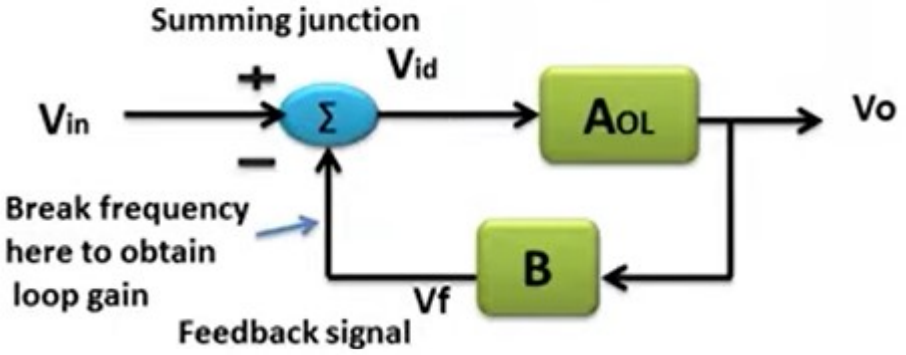
Where $f_d < f_1 < f_2 < f_3$

CIRCUIT STABILITY OF OP AMP

Group of circuit connected together as a system is said to be stable if output reach a fixed value in a finite time , and circuit system is said is unstable if output increase with time .

Common method is routh hurwitz criteria , graphic method is bode plots.

CIRCUIT STABILITY OF OP AMP



Open loop gain op amp is complex quantity and a function of frequency . We represent it by $A_{OL}(f)$

$$A_{OL} = \frac{Vo}{vin} \qquad \text{If } Vf = 0$$

close loop voltage gain A_F

$$A_F = \frac{Vo}{vin} \qquad A_F = \frac{A_{OL}}{1 + (A_{OL})(B)}$$

System stability determine as methods =

Method 1 = determine the phase angle when the magnitude of (AOL)(B) is 0dB or 1 if phase angle is > -180^0 system is stable, some systems magnitude may never be 0 dB

Method 2 = determine the magnitude of (AOL)(B) when phase angle is -180^0 if magnitude in –ve decibels system is stable, some systems system may never reach -180^0

SLEW RATE

Slew rate =

It is define as maximum rate of change of output voltage per unit time it show in per microsecond . Slew rate change with the change of voltage gain .

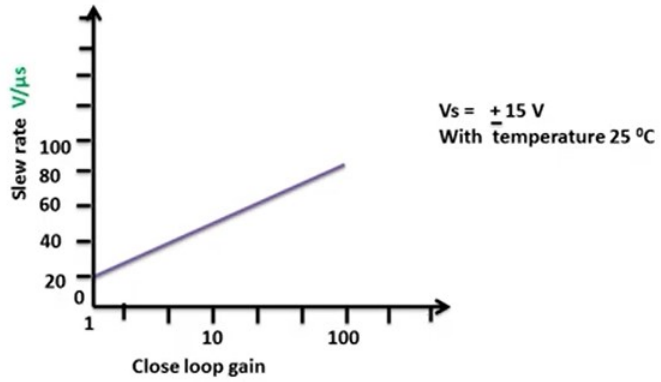
$SR = dVo/dt$ | Max V/µs

For example 1 V/µs slew rate means output rise and fall no faster then 1 V in every microsecond .

Op amp are available with slew ate from 0.1V/µs to well about 1000 V/µs national semiconductor LH0063C has slew rate 6000 V/µs

It is specified for unity gain and measure by applying a step input voltage .

Slew rate improve with higher close loop gain and dc supply voltage.



Slew rate with close loop gain

Slew Rate (SR):

Another important frequency related parameter of an op-amp is the slew rate. **Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/µs.** It indicate how fast op amp respond to change in input.

Effect of Slew rate: **The time taken for output will be change from +Vm to-Vm after input change. It is called Slew rate.** From the fig. It takes some time to change +Vm to –Vm and –Vm to +Vm. Because of delay the output gets distorted.

If slew rate high output cannot distorted (output will change quickly with time without delay) . It is less the output will be distorted.

The time taken to change output from +Vm to –Vm and –Vm to +Vm, is depends upon slew rate.

Effect of slew rate:

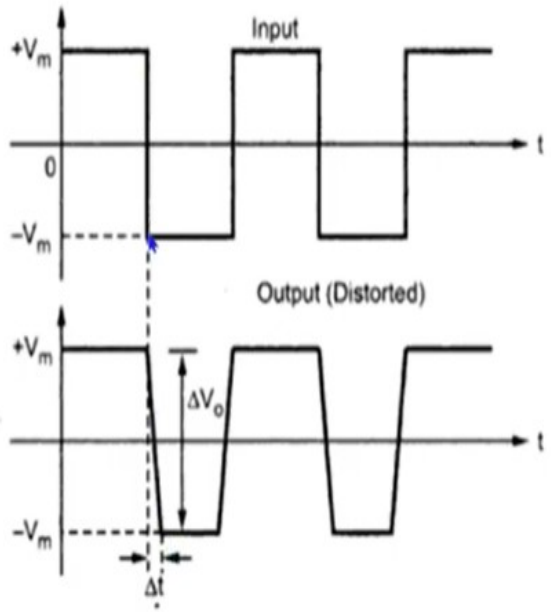


Fig. 2.40 Effect of slew rate

Reason for Slew rate: There is usually a capacitor within or outside an op-amp to prevent oscillation. This capacitor which prevents the o/p voltage from fast changing input.

The rate at which the voltage across the capacitor changes is given by

$$\frac{dV_c}{dt} = \frac{\mathrm{I}}{\mathrm{C}} \qquad Capacitor\ current(I_c) = C\frac{dV_c}{dt}$$

I is the Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors.

For 741 IC, the maximum internal capacitor charging current is limited to about 15μ A. So the slew rate of 741 IC is

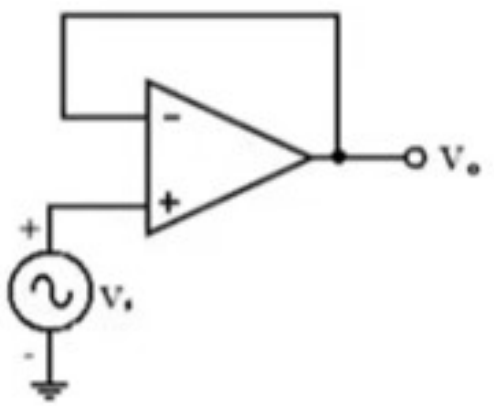
$$SR = \left(\frac{dV_c}{dt}\right)_{max} = \frac{(\mathrm{I})_{\mathrm{max}}}{\mathrm{C}}$$

For a sine wave input, the effect of slew rate can be calculated as consider voltage follower . The input is large amplitude, high frequency sine wave .

For voltage follower, the gain should be unity.
Output voltage is equal to input voltage.

If input $V_s = V_m$ Sinwt then
Output $V_0 = V_m$ Sinwt .
The rate of change of output is given by

$$\frac{dV_0}{dt} = V_m w \, Coswt$$



voltage follower circuit

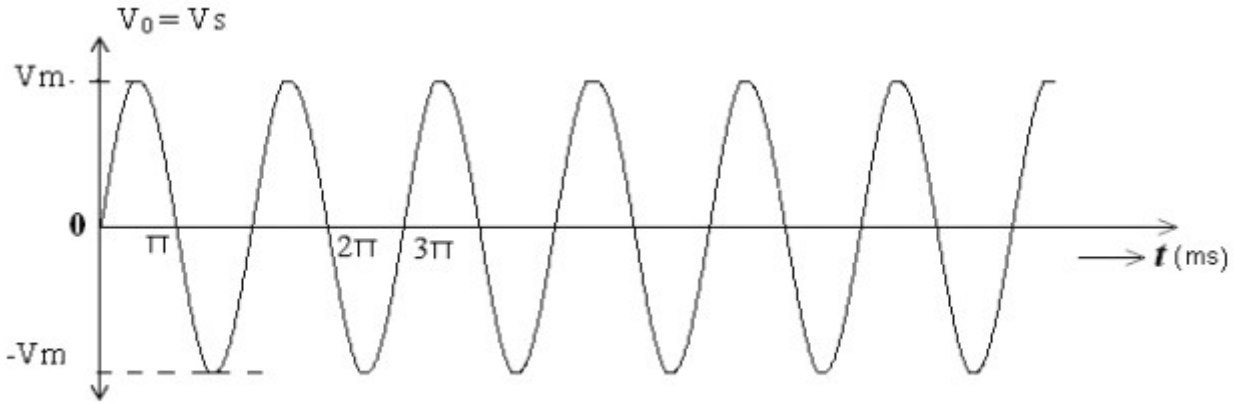
The max rate of change of output is obtained when coswt =1

$$Slew\ Rate = \left(\frac{dV_c}{dt}\right)_{max} = wV_m = 2\pi f V_m \quad (v/ms)$$

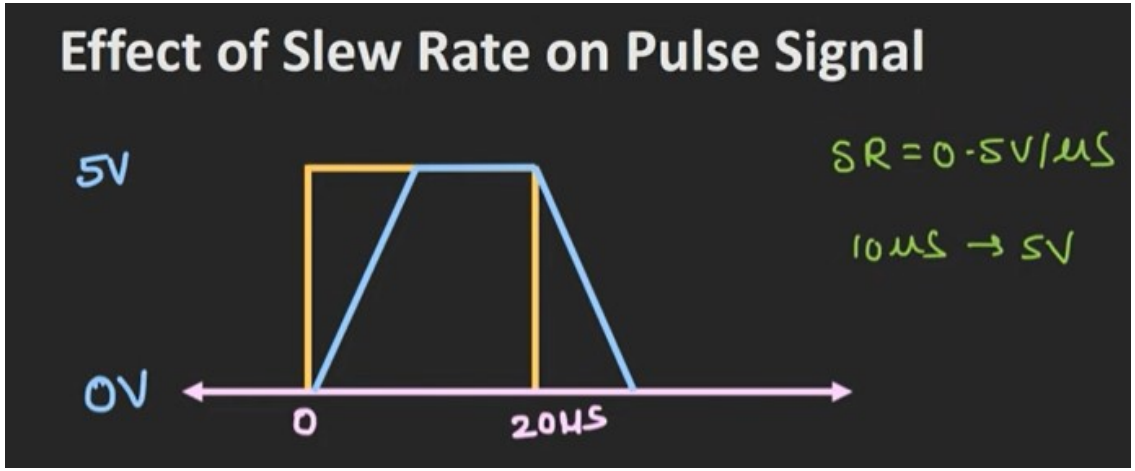
Thus the maximum frequency f_{max} at which we can obtain an undistorted output volt of peak value V_m is given by

$$f_{max} = \frac{SR}{2\pi V_m}$$

Where fmax is called the full power response(bandwidth). It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.



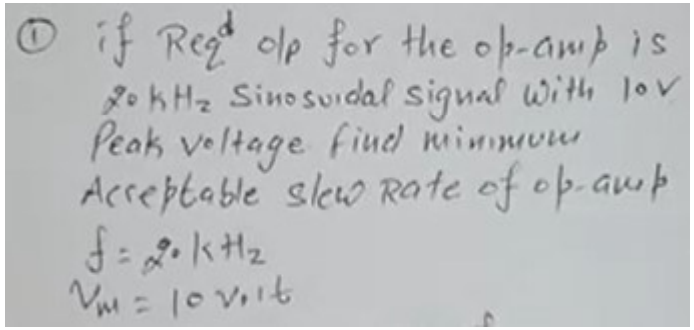
Input and Output Waveforms

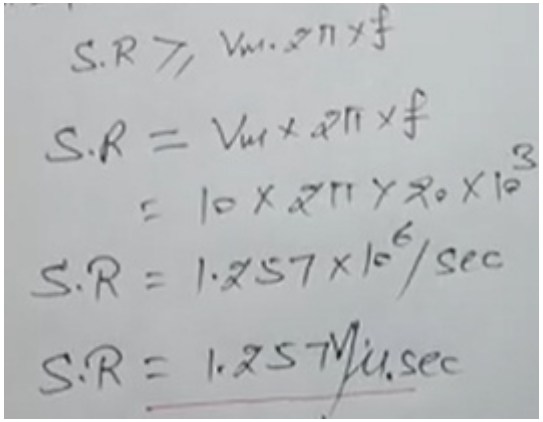


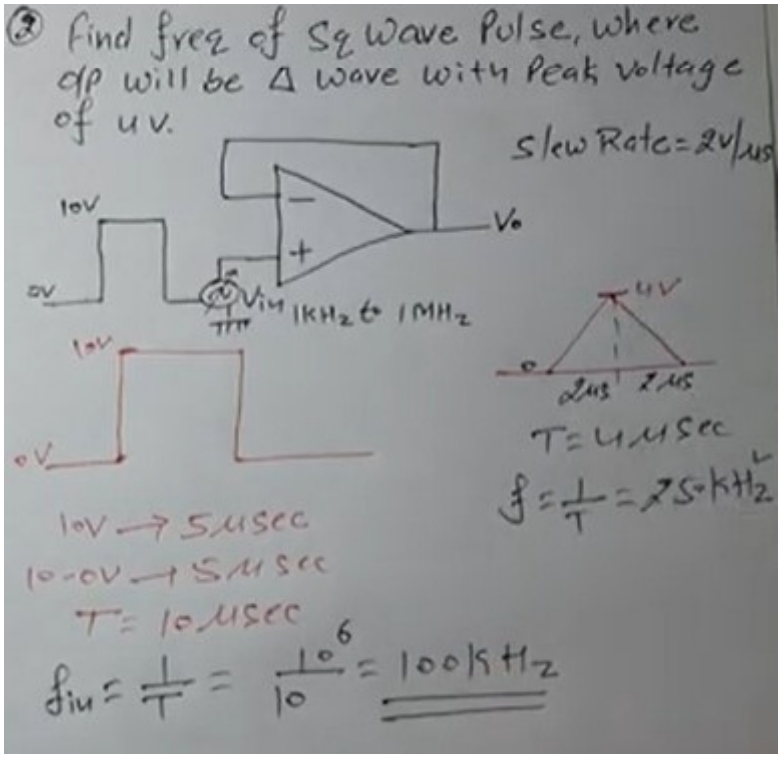
An operational amplifier is required to amplify a signal with a peak voltage of 5 volts at a frequency of 20kHz. Find out a slew rate.

Given data: $V_m = 5volts,\ f_m = 20kHz$

$$S = 2\pi f_m V_m$$
$$= 2 * 3.14 * 20 * 10^3 * 5$$
$$= 628 * 10^3$$
$$S = 628000V/S \ or \ 0.628V/\mu S$$







What is the largest sine wave output voltage (in Volts) possible at frequency of 1 MHz when an Op-amp has slew rate of 10 V/μs?

Slew Rate :

The maximum rate of change of output voltage .

Unit : volts per second

It decides maximum operable frequency of opamp.

let V_{in} = A sin $2\pi f_m t$

$V_0 = V_{in} =$ **A sin** $2\pi f_m t$

Slew Rate = $\frac{dV_0}{dt} = A.2\pi f_m \cos 2\pi f_{mt}$

$\frac{dV_0}{dt}|_{max} = A.2\pi f_m$

Calculation :

$10\ V/\mu s = A \times 2 \times \pi \times 10^6$

$10\ V/10^{-6} = A \times 2 \times \pi \times 10^6$

$A = 5 / \pi$

An op-amp amplifier of gain 10 is used to amplify a sinusoidal signal with a peak amplitude of 0.5 V and frequency of 25kHz. What should be the minimum slew rate of the op-amp used ?

Concept:

When the input is a sinusoid given as:

$V_i(t) = A_m \sin(2\pi f_m t)$

Let, the gain of OPAMP is 'A_v', the output is given as:

$V_o(t) = A_v A_m \sin(2\pi f_m t)$

The rate of change of output:

$$\frac{dV_o}{dt} = A_v A_m \cos(2\pi f_m t)$$

The maximum rate of change = $|A_v A\, 2\pi f_m \cos(2\pi f_m t)|_{max}$

$$\frac{dV_o}{dt}\Big|_{max} = A_v A_m\, 2\pi f_m = Slew\ Rate$$

Calculation:

Slew rate : $10 \times 0.5 \times 2\pi \times 25 \times 10^3 = 785 \times 10^3$ V/s

= 0.785 V/μs

What is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.2 V in 10 µs with slew rate of op-amp SR = 2 Vµs?

The equation for the slew rate is given by,

$$S = \frac{dV_0}{dt}|_{maximum} Volts/\mu sec$$

Here,

$$S = \frac{dV_0}{dt} = 2$$

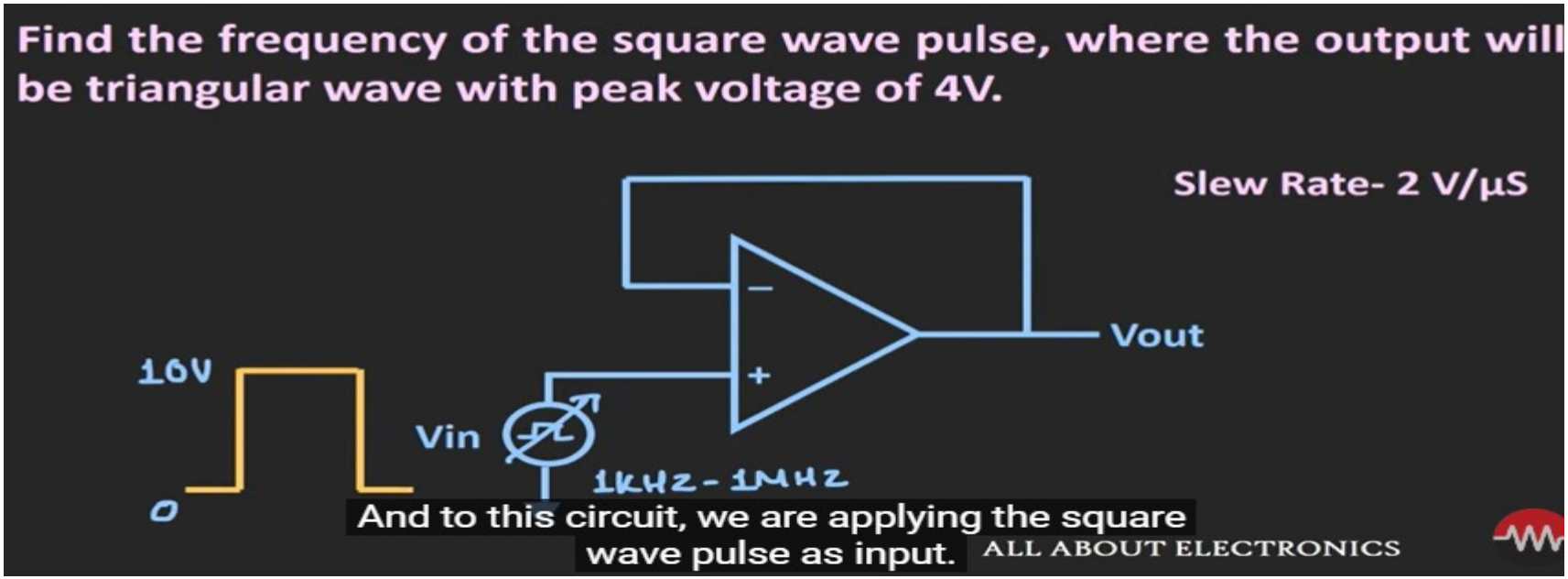
it is given that the input signal varies by 0.2 V in 10 µs which can be written mathematically as,

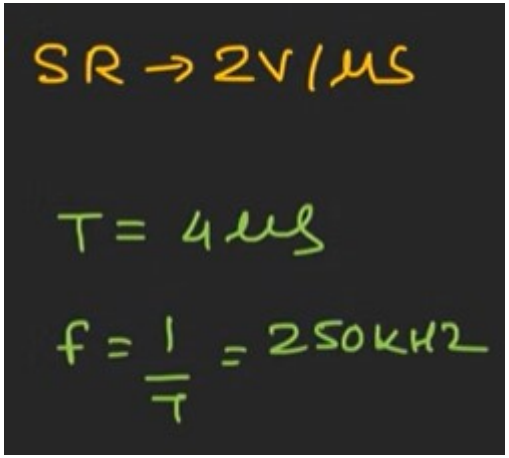
$$\frac{dV_i}{dt} = \frac{0.2}{10} = 0.02\ per\ \mu sec$$

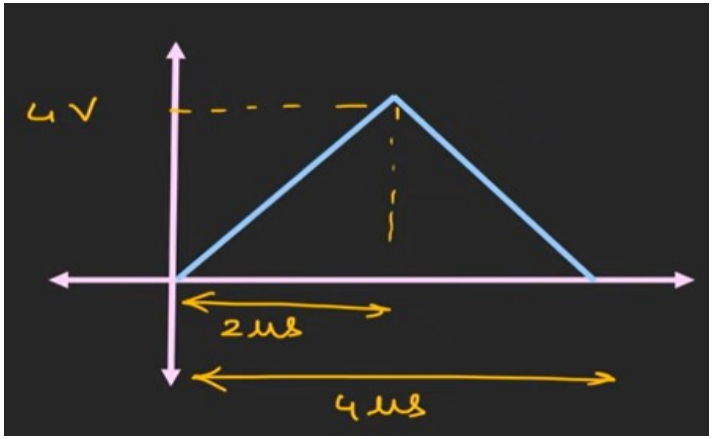
we that voltage gain is given by= $\frac{dV_o}{dV_i}$

$$= \frac{(\frac{dV_o}{dt})}{(\frac{dV_i}{dt})}$$

$$= \frac{2}{0.02} = 100$$







If SR = 2V/µs, To reach peak value of 4 V, Time required is 2 µs, similarly peak to zero volts is 2 µs, total time is 4µs. Hence f=1/T =1/4 µs =250khz.

20 **Op-amp 741:**

The IC 741 is high performance monolithic op-amp IC .It is available in 8 pin, 10 pin or 14 pin configuration. It can operate over a temperature of -55 to 125 centigrade.

Features of IC-741

- No frequency compensation required.
- Short circuit protection provided.
- Offset voltage null capability.
- Large common mode and Differential voltage range.
- No latch up.
- No External frequency compensation is required
- Short circuit Protection
- Low Power dissipation

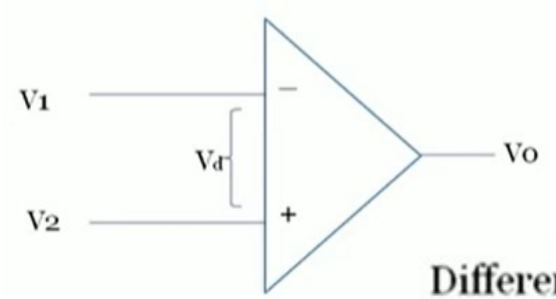
Specifications

The following are the basic specifications of IC 741:
Power Supply: Requires a Minimum voltage of 5V and can withstand up to 18V
Input Impedance: About 2 MΩ
Output impedance: About 75 Ω
Voltage Gain: 200,000 for low frequencies (200 V / mV)
Maximum Output Current: 20 mA
Recommended Output Load: Greater than 2 KΩ
Input Offset: Ranges between 2 mV and 6 mV
Slew Rate: 0.5V/μS (It is the rate at which an Op-Amp can detect voltage changes)
The high input impedance and very small output impedance makes IC 741 a near ideal voltage amplifier.

Differential Mode gain, Ad

Differential mode→ Vin1≠Vin2

$$V_d = V_1 - V_2$$

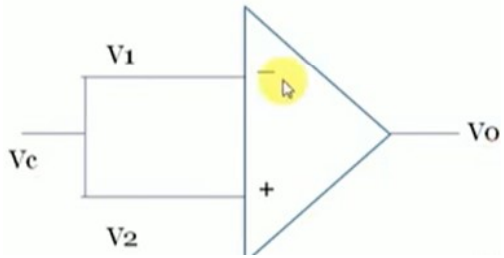


$V_o = A_d V_d$ Where Vd=V2-V1

Differential mode gain, $A_d = \frac{V_o}{V_d}$

Differential mode gain in dB, $A_d = 20 \log_{10}\left(\frac{V_o}{V_d}\right)$ in dB

Common Mode gain, Ac



Common mode→ Vin1=Vin2

$V_o = A_c V_c$

Where $V_c = \frac{V_1+V_2}{2}$ Average of two input signals

Common mode gain, $A_c = \frac{V_o}{V_c}$

Common mode gain in dB, A_c (in dB) $= 20 \log \left(\frac{V_o}{V_c}\right)$

Finally, the total output of differential amplifier is

Vo=Vo(differential mode)+Vo(common mode) $V_o = V_d A_d + V_c A_c$

Common mode Rejection Ratio (CMRR):

- The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called Common Mode Rejection Ratio.
- Mathematically, CMRR is defined as the ratio of differential voltage gain to common mode voltage gain.

$$CMRR, \rho = |Ad/Ac|$$

$$\text{CMRR in dB} = 20 \log \left| \frac{A_d}{A_c} \right| \text{ dB}$$

The output voltage, V_o can be expressed interms of CMRR as below: We know that, $V_o = V_d A_d + V_c A_c$

$$V_o = A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d}\right)$$

$$V_o = A_d V_d \left[1 + \frac{1}{\rho} \cdot \frac{V_c}{V_d}\right]$$

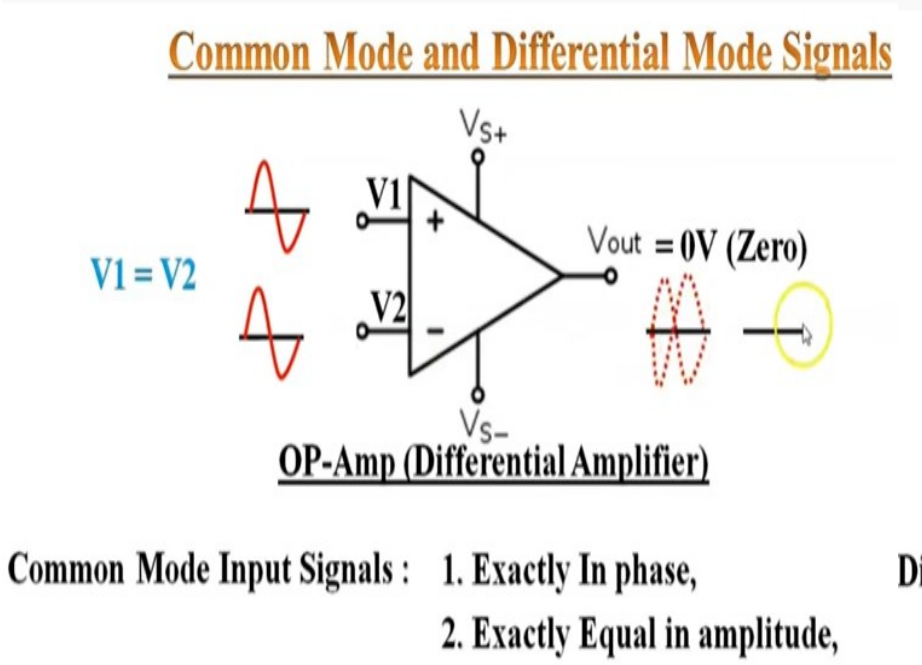
$V_o = A_d V_d$ For higher values of ρ

Common mode rejection ratio (CMRR):

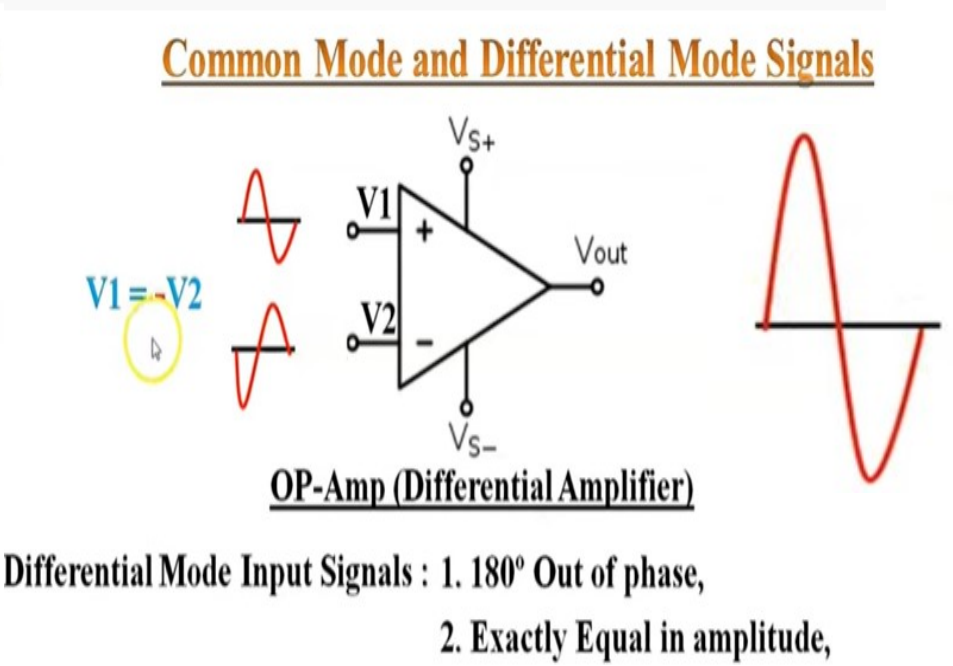
The ability of a differential amplifier to reject common mode signal is described in terms of **Common mode rejection ratio.**

CMRR is defined as the ratio of differential voltage gain (A_d) to the common mode voltage gain (A_{cm}).

$$\mathbf{CMRR = A_d / A_{cm}}$$

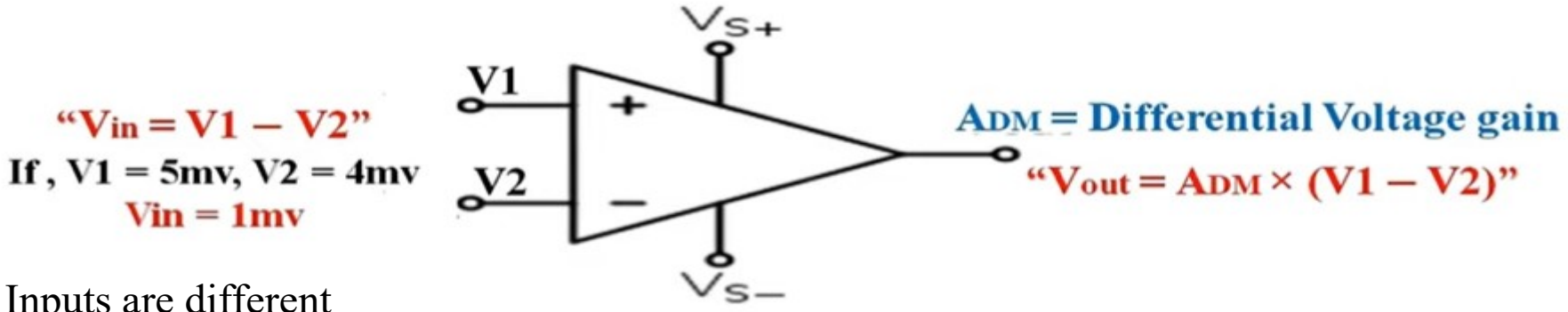


Common Mode Input Signals : 1. Exactly In phase,
2. Exactly Equal in amplitude,



Differential Mode Input Signals : 1. 180° Out of phase,
2. Exactly Equal in amplitude,

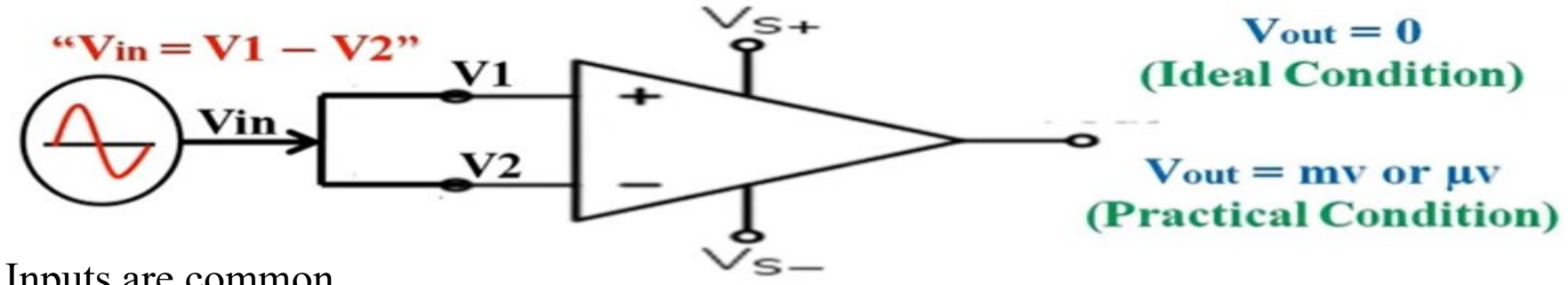
The amplifier amplify the differential mode signals and rejects the common mode signals.



Inputs are different

OP-Amp Differential mode configuration

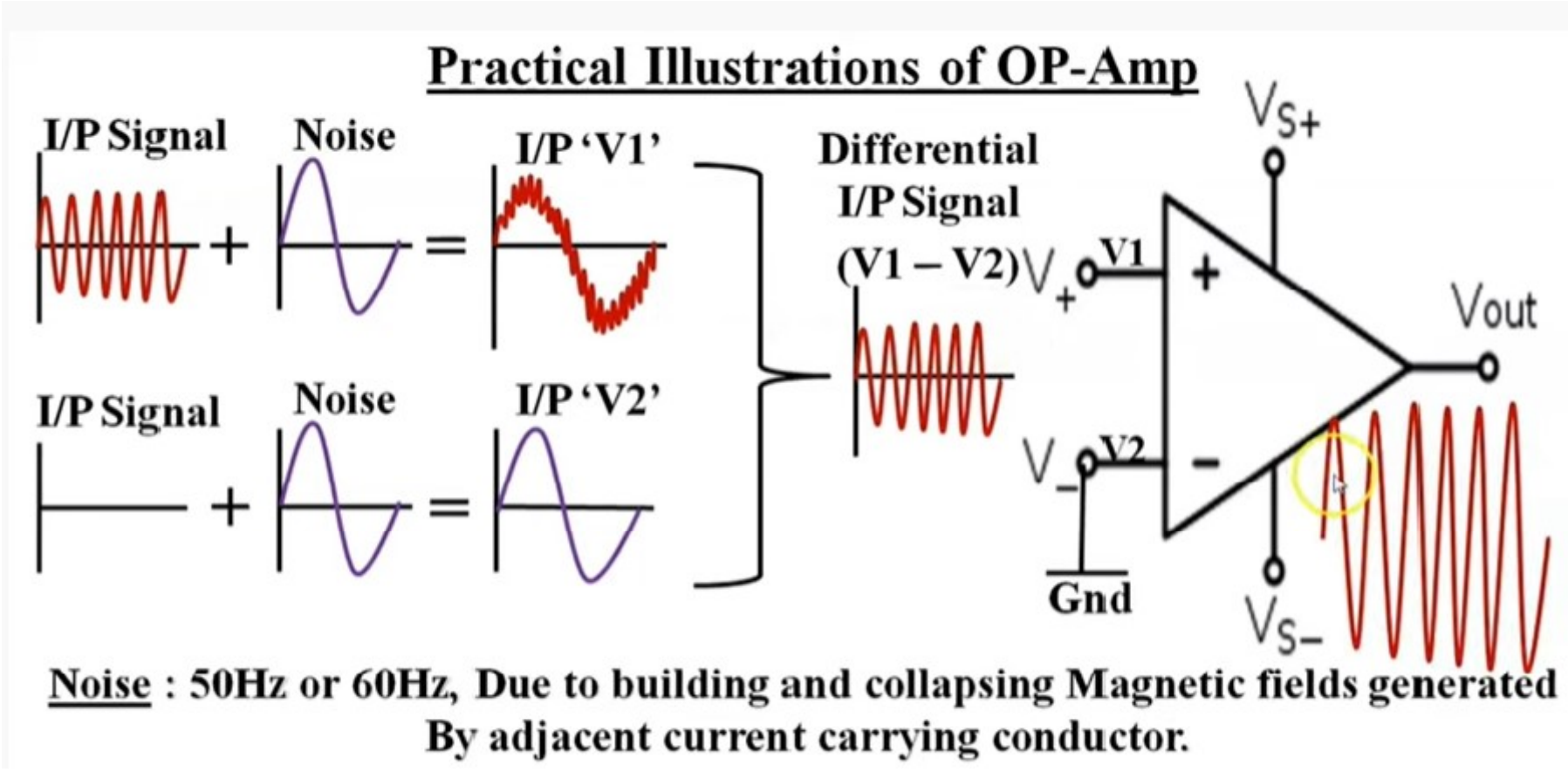
If ADM = 10,000 then,
Vout = 10,000 × 1mv = 10V



Inputs are common

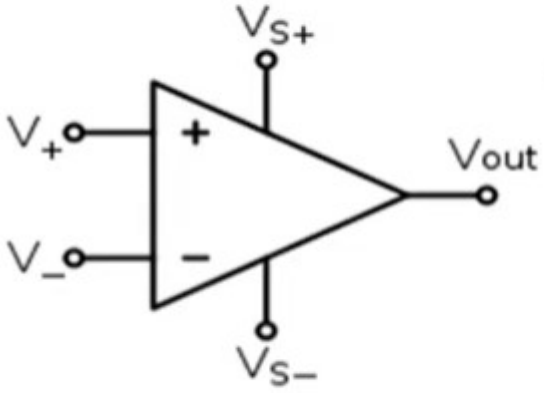
OP-Amp Common Mode Configuration

ACM = Common mode Voltage gain
ACM = 0 (Ideal condition)
ACM < 1 (Practical condition)



In the above fig input signal V1 and V2 are different magnitude and noise present in both input terminals are same (common). Hence differential input signal Vd=V1-V2 will amplify and noise present in both input terminals is same, so it can cancel and output will be amplified output without distortion.

Common Mode Rejection Ratio



OP-Amp (Differential Amplifier)

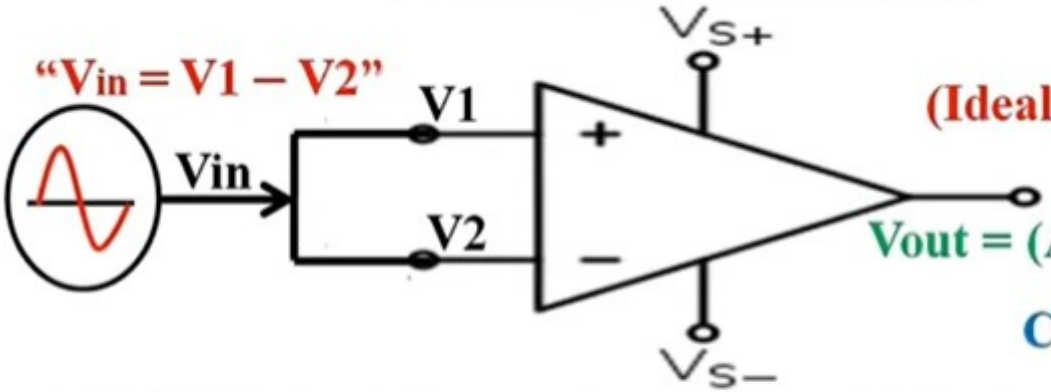
Should have High Differential Voltage gain(A_{DM})
Very Low Common mode Voltage gain (A_{CM})
The Ratio of "$A_{DM} / A_{CM} = CMRR$"

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

$$CMRR_{dB} = 20 \log_{10} \frac{A_{DM}}{A_{CM}}$$

$$= 20 \log_{10} CMRR$$

Importance of CMRR



(Ideal) "$V_{out} = A_{DM} \times V_{in}$"

Practical :

$V_{out} = (A_{DM} \times V_{in}) + (A_{CM} \times V_{in})$

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

1. CMRR is the ability to reject Common Mode signals
2. The larger the CMRR, better at eliminating Common Mode signals

EX : If, $A_{DM} = 1500$, $A_{CM} = 0.01$,

Then CMRR = 1500 ÷ 0.01 = 150,000,

This means Differential O/P is 150,000 times greater than Common mode O/P

Common mode signals are undesired signals caused by external interference,

The CMRR of an OP-Amp indicates, its ability to remove such unwanted signals.

unwanted signals now we will solve some

Examples and Solutions

Ex-1 : **A differential amplifier has an output of 1V with a differential Input of 10mV, and an output of 5mV with a common mode Input of 10mV, Find out CMRR in dB ?**

Sol : **Differential Input = 10mV, Differential Output = 1V**

Differential Gain, A_{DM} = 1V/10mV = 100 (Output / Input)

Common mode Input = 10mv, Common mode Output = 5mv

Common mode Gain, A_{CM} = 5mV/10mV = 0.5 (Output / Input)

$$\text{CMRR} = \frac{A_{DM}}{A_{CM}} \qquad \text{CMRR}_{dB} = 20 \log_{10} \frac{A_{DM}}{A_{CM}}$$

$$\text{CMRR}_{dB} = 20 \log_{10} \frac{100}{0.5} = 46\text{dB}$$

CMRR is 100 db. Input common mode voltage is 12v. Differential voltage gain is 4000. Calculate output common mode voltage

Calculation:

Given: A_d = 4000,

CMRR = 100 db

⇒ CMRR in db = 20 log |CMRR| = 100

⇒ CMRR = 100000

$100000 = \frac{4000}{A_c}$

Input common-mode voltage is 12 V

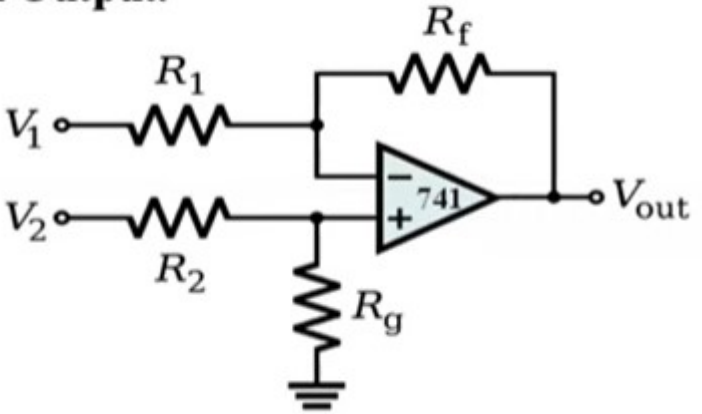
⇒ V_c

Output common-mode voltage of Op-Amp will be:

$V_o = A_c V_c$

= .04 × 12 = .48 V

Ex-2 : The differential amplifier shown in figure has a voltage gain of 150, CMRR of 90dB, The Input signals, V1 = 50mV, V2 = 100mv and Noise on each Input = 1mV, Find out (1) The Output signal, (2) The Noise on Output.



Sol : Output signal, Vout = ADM (V1-V2)

$= 150\ (100mV - 50mV) = 7.5V$

$$CMRR_{dB} = 20 \log_{10} \frac{A_{DM}}{A_{CM}}$$

$$90_{dB} = 20 \log_{10} \frac{150}{A_{CM}}$$

$$31623 = \frac{150}{A_{CM}}$$

$$A_{CM} = \frac{150}{31623} = 0.0047 = 4.7 \times 10^{-3}\ (4.7\ mV)$$

Noise on Output $= A_{CM} \times 1mV = 4.7 \times 10^{-3} \times 10^{-3} = 4.7 \times 10^{-6}\ (4.7\mu V)$

A given op-amp has an open loop gain of 110 dB and a CMRR rating of 100 dB. What should be the open loop common mode gain of this op-amp ?

Concept:

CMRR (Common mode rejection ratio) is defined as the ratio of differential-mode voltage gain (A_d) and the common-mode voltage gain (A_C).

Mathematically, in dB this is expressed as:

$$CMRR(dB) = 20 \log \left| \frac{A_d}{A_c} \right|$$

A_d = Differential gain

A_c = Common mode gain

Using the property of log, we can write:

CMRR (dB) = 20log (A_d) - 20log (A_c)

CMRR (dB) = A_d(dB) - A_c(dB)

Calculation:

Given:

A_d(dB) = 110 dB

CMRR (dB) = 100 dB

We can write:

CMRR (dB) = A_d(dB) - A_c(dB)

100 dB = 110 dB - A_c(dB)

A_c(dB) = 110 dB - 100 dB

A_c(dB) = 10 dB

Op-Amp Applications:

Op –amp is a very high gain differential amplifier. Gain of op amp is 10^5 to 10^6 ·

Small differential input voltage between input terminals of op amp, output voltage gets saturated towards positive or negative .

A circuit is said to be **linear, if there exists a linear relationship between its input and the** output. Similarly, a circuit is said to be **non-linear, if there exists a non-linear relationship** between its input and output.

Op-amps can be used in both linear and non-linear applications. The following are the basic applications of op-amp:

- Inverting Amplifier
- Non-inverting Amplifier
- Voltage follower
- Integrator and differentiator
- Differential amplifier
- Instrumentation amplifier
- Analog multiplier
- V to I, I to V converters
- Rectifiers
- Sample and Hold circuits
- Log and Anti log amplifier

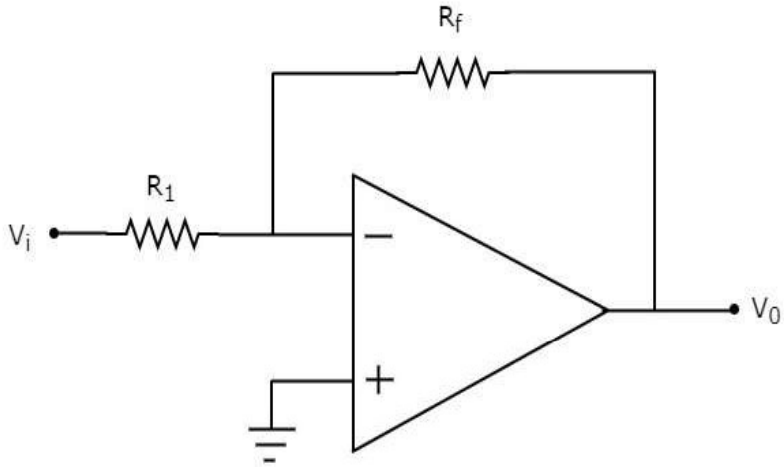
Ideal Characteristics of op-amp:

Characteristics Parameter	Ideal value	Practical value
Voltage Gain (Av)	∞	≈ 10^6
Input Resistance (Ri)	∞	≈ 1 MΩ
Output Resistance (R0)	0	≈ 10 Ω to 100 Ω
Bandwidth (B.W)	∞	≈ 1 MHz
Slew Rate (S.R)	∞	≈ 80 V/μs

Inverting Amplifier

An inverting amplifier, the input(ac or dc) applied to inverting terminal through a resistor $R1$ and –ve feedback given through R_f, and produces its amplified output with 180^0 phase shift w.r.t input. This amplifier not only amplifies the input but also inverts it (changes its sign).

Note that for an op-amp, the voltage at the inverting input terminal is equal to the voltage at its non-inverting input terminal.
Physically, there is no short between those two terminals but **virtually they are in short with each other.**
Virtual ground concept is applicable for –ve feedback present in circuit.



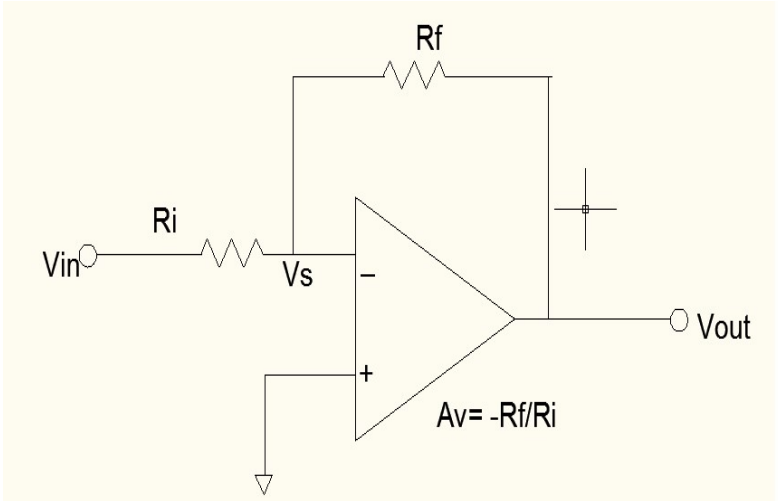
inverting amplifier

In the circuit shown above, the non-inverting input terminal is connected to ground. That means zero volts is applied at the non-inverting input terminal of the op-amp. According to the **virtual short concept, the voltage at the inverting input terminal of an** op-amp will be zero volts. The virtual ground applicable for –ve feedback present.

Gain of amplifier is control by –ve feedback and amplifier operates in linear region not enter in saturation region

From the circuit, when a voltage Vi is applied to its input, the current I_1 is flowing through R_i (input resistor), and also the current I_f is flowing through R_f (feedback resistor).

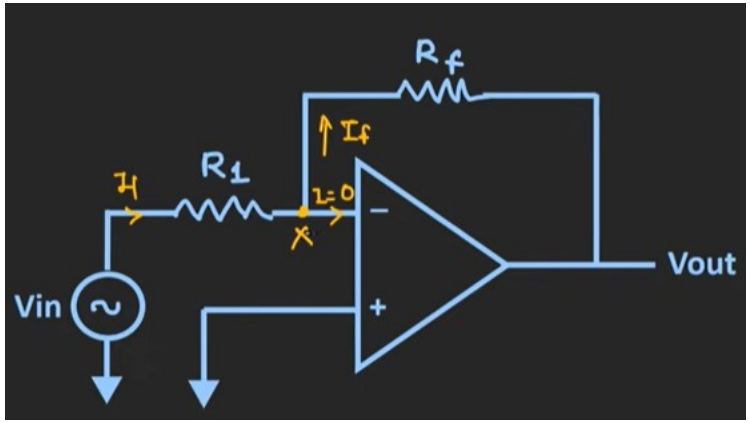
Since its input impedance is high, no current enters into an operational amplifier.



I_1 – Current flows through Ri

I_f – Current flows through Rf

Applying Kirchhoff's current law at the inverting node,



$$i_1 = i_f$$

$$\frac{V_i - V_s}{R_i} = \frac{V_s - V_o}{R_f}$$

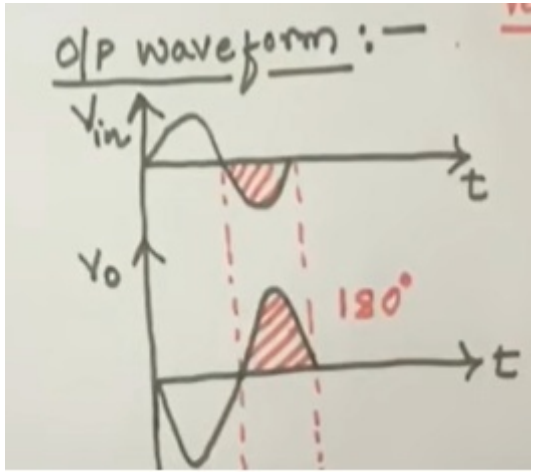
Vs = o, because it is virtual ground.

If V_s=0 the above equation is $\frac{V_i}{R_i} = -\frac{V_0}{R_f}$

$$V_0 = -\frac{R_f}{R_i} \times V_i$$

$$= \frac{R_f}{R_i} \times (-V_i)$$

$$\text{Voltage gain, } A_v = \frac{V_0}{V_i} = -\frac{R_f}{R_i}$$



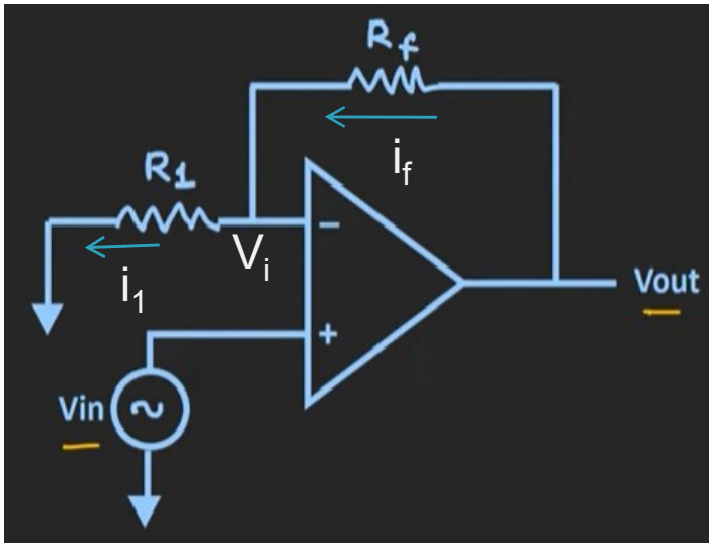
The input voltage is amplified in accordance with the values (ratio) and R_i, and also inverted.

The ratio of the output voltage $V0$ and the input voltage Vi is the voltage-gain or gain of the amplifier. Therefore, the **gain of inverting amplifier is equal to $-Rf$ / $R1$.**

Note that the gain of the inverting amplifier is having a **negative sign. It indicates that** there exists a 180^0 phase difference between the input and the output.

NON-INVERTING AMPLIFIER:

A non-inverting amplifier, the input applied to its non-inverting terminal and produces its amplified output. In this amplifier Output and input are in phase. As the name suggests, this amplifier just amplifies the input, without inverting or changing the sign of the output.



The input voltage Vi is directly applied to the non-inverting terminal. According the characteristics of an op-amp, the applied input voltage Vi is also developed at the inverting input terminal.

According to the **virtual short concept, the voltage at the inverting input terminal of an** op-amp is same as that of the voltage at its non-inverting input terminal.

Applying Kirchhoff's current law $I_1 = I_f$

$$\frac{V_i}{R_1} = \frac{V_0 - V_i}{R_f} \Rightarrow \frac{V_0}{R_f} = \frac{V_i}{R_1} + \frac{V_i}{R_f} \Rightarrow \frac{V_0}{R_f} = V_i\left(\frac{1}{R_1} + \frac{1}{R_f}\right) \Rightarrow \frac{V_0}{V_i} = R_f\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$Voltage\ gain\ (A_V) = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

The output voltage is always in phase with the input. The gain of this amplifier also depends upon the external connected components of Rf and Ri.

Difference between Inverting Amplifier and Non-inverting Amplifier:

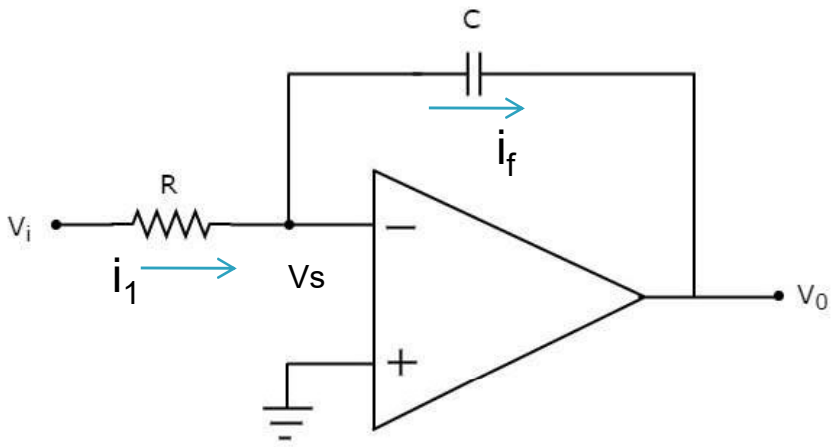
Inverting Amplifier	**Non-inverting Amplifier:**
The input is given to the inverting input terminal of the op-amp.	The input is given to the non-inverting input terminal of the op-amp.
It gives an inverted output.	It gives an output which is in phase with the input signal.
The gain of the inverting amplifier, when used with a negative feedback, is directly proportional to the ratio of the feedback resistor/ input resistor.	The gain of the non-inverting amplifier is also proportional to the ratio of the feedback resistor/ input resistor but with an intercept value.

INTEGRATOR: Op amp used a integrator.

An integrator circuit integrates the input signal with respect to time (frequency).

An integrator is an electronic circuit that produces an output that is the integration of the applied input.

An op-amp based integrator produces an output, which is an integral of the input voltage applied to its inverting terminal. The **circuit diagram of an op-amp based integrator is** shown in the following figure:



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.

According to **virtual short concept, the voltage at the inverting input terminal of op-amp** will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The charge on a capacitor C, when a supply voltage of V applied is Q = CV.
In general, the current through the capacitor,

$$I_c = \frac{dQ}{dt} = \frac{dCV}{dt} = \frac{CdV}{dt}, \text{since C is constant}$$

By using Kirchhoff's current law in the circuit.

$$i_1 = i_f$$

$$\frac{V_i - V_s}{R} = C\,\frac{dV}{dt}$$

$$\frac{V_i - V_s}{R} = C\,\frac{d(V_s - V_0)}{dt}$$

Since V_s=0 (it is virtual ground)

$$\frac{V_i}{R} = -C\,\frac{dV_0}{dt} \quad \Rightarrow \quad \frac{dV_0}{dt} = -\frac{V_i}{RC}$$

Integrating on both sides with respect to time

$$V_0 = -\frac{1}{RC}\int V_i(t)\,dt + V_k(0)$$

Where Vk(0) is the initial voltage produced at the output.

Note: The output voltage, V_0 is having a negative sign, which indicates that there exists 180^0 phase difference between the input and the output.

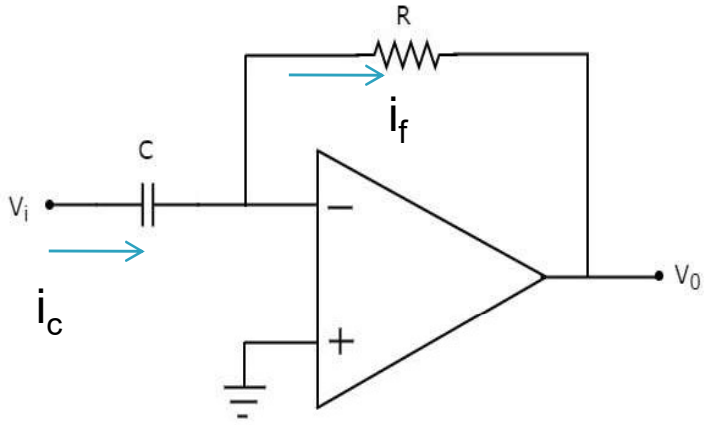
- For a square wave input, it produces triangular output waveform.
- For a sine wave input, it produces cosine output waveform.

The integrator is most commonly used in analog computers and A/D converters.

DIFFERENTATOR:

It produces the output signal, which is the **Differentiation** *of input signal Vi. It produces a output voltage which is directly proportional to the rate-of-change with respect to time input voltage's.*

An op-amp based differentiator produces an output, which is equal to the differential of input voltage that is applied to its inverting terminal.
The **circuit diagram of an op-amp** based differentiator is shown in figure:



If the resistor and capacitor of an integrator are interchanged, it will act as differentiator.

The charge on a capacitor C, when a supply voltage of V applied is Q=CV.

According to the **virtual short concept, the voltage at the inverting input terminal of op amp** will be equal to the voltage present at its non-inverting input terminal.
So, the voltage at the inverting input terminal of op-amp will be zero volts.

By using Kirchhoff's current law

$$i_c = i_f$$

$$\frac{C\, d(V_i - V_s)}{dt} = \frac{V_s - V_0}{dt}$$

$V_s = 0$, because it is a virtual ground;

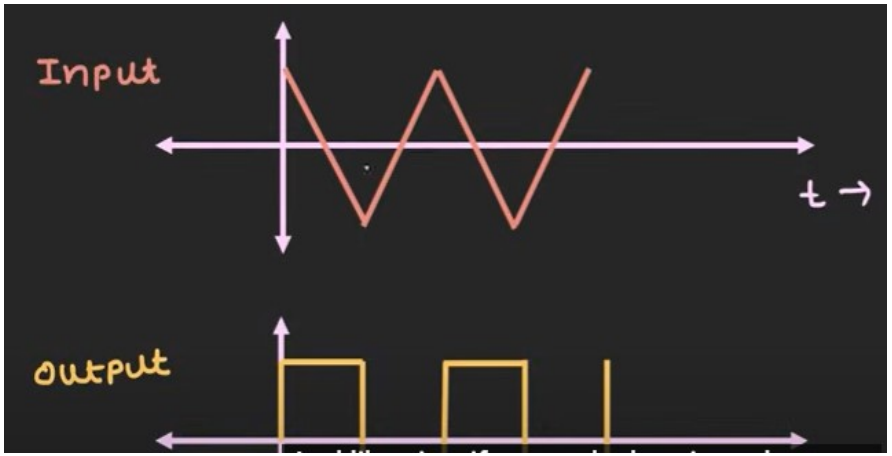
$$\frac{CdV_i}{dt} = -\frac{V_0}{R} \quad \Rightarrow \quad \frac{V_0}{R} = -\frac{CdV_i}{dt} \quad \Rightarrow \quad V_0 = -RC\frac{dV_i}{dt}$$

Thus, the op-amp based differentiator circuit shown above will produce an output, which is the differential of input voltage Vi, when the magnitudes of impedances of resistor and capacitor are reciprocal to each other.

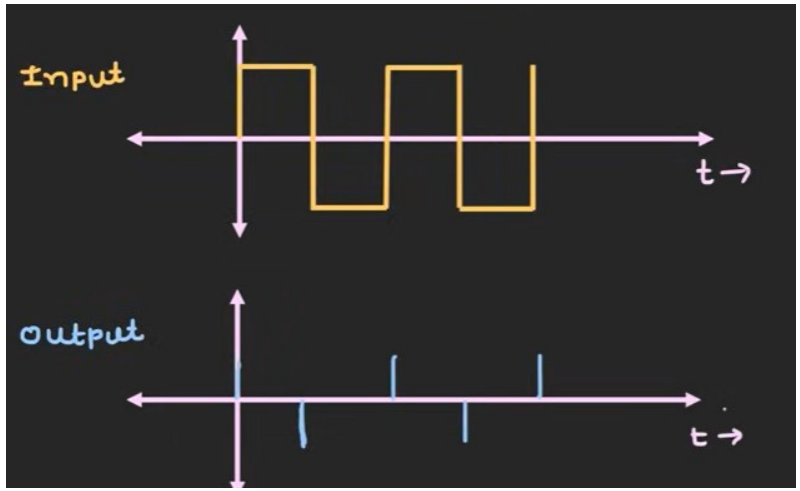
Note that the output voltage V_0 is having a **negative sign, which indicates that there** exists a 180^0 phase difference between the input and the output.

The output signal is the differentiation of input signal with respect to time.

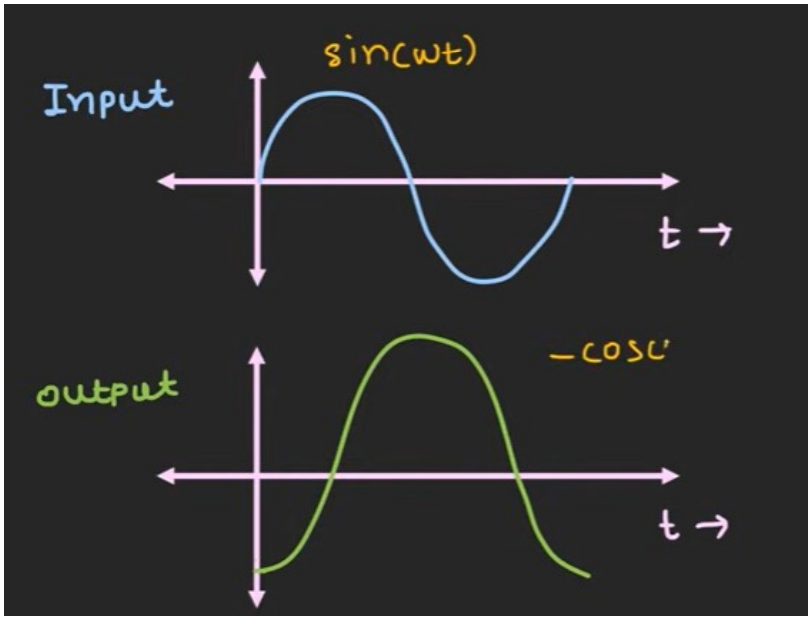
- For a square wave input, it produces spike output.
- For a cosine wave input, it produces sine wave output.
- For a triangular wave input, it produces square wave output.



Triangular wave input, Produce Square as output

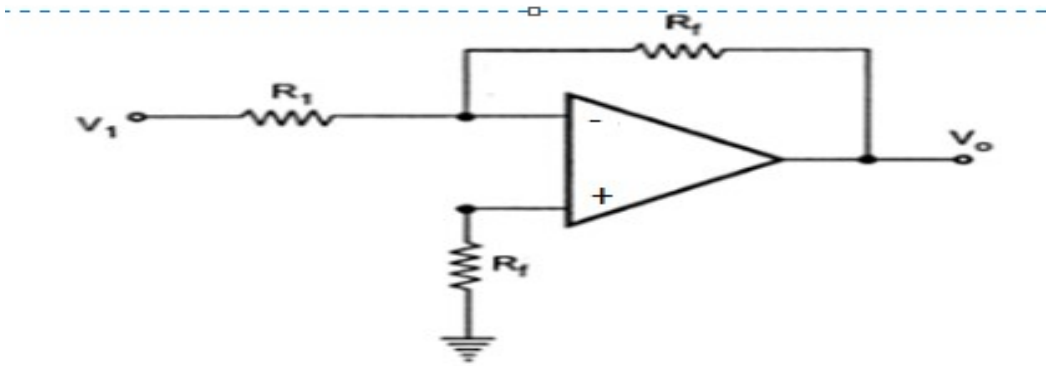


Square wave input, Produce Spike as output



Sine wave input, Produce Cosine output

Design an amplifier with a gain of -10 and input resistance of 10kΩ.



Gain A= $(V_o/V_i) = (R_f/R_i)$

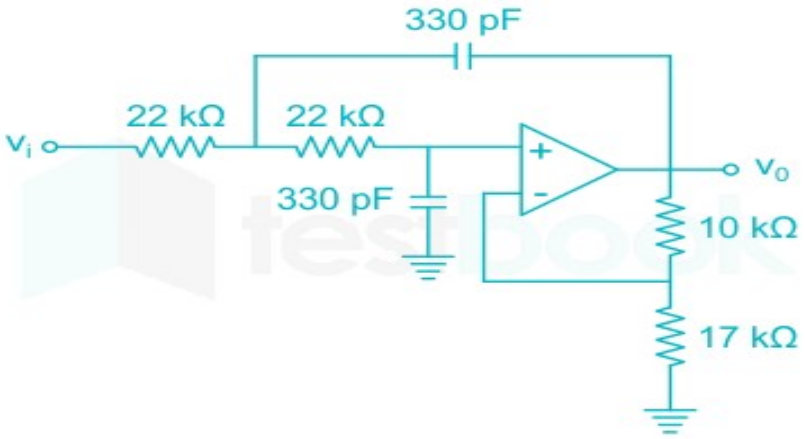
$-10 = (R_f/10K\Omega)$

Feed back resistance, $R_f = 100\ K\Omega$.

In a non-inverting OPAMP, if R1 = 20 K ohms and Rf = 200 K ohms, then find the gain of the amplifier.

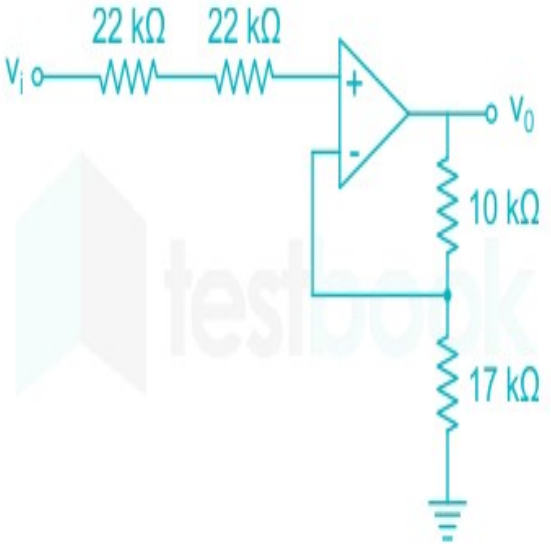
$$Voltage\ gain\ (A_V) = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

Consider the circuit shown below. The dc gain v_0/v_i is



Calculation:

For dc, all capacitors are open circuited then op-amp is a non-inverting amplifier



$$Voltage\ gain\ (A_V) = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

$$v_0 = \left(1 + \frac{10}{17}\right) v_i \Rightarrow \frac{v_0}{v_i} = 1.58$$

EX.1: Determine the output voltage of a differential amplifier for the input voltages of 300μV and 240μV.The differential gain of amplifier is 5000 and the value of CMRR is I) 100 II) 10^5.

$V_{CM} = (1/2)\ (V1+V2)$, $V_d = V_1 - V_2$ $CMRR = A_{DM}/A_{CM}$, We know that, $V_0 = V_d A_d + V_c A_c$

$A_{DM} = V_0/V_d$, $A_{CM} = V_0/V_{CM}$

What is the maximum frequency for a sine wave output voltage of 10 V peak with an Op-amp whose slew rate is 1 V/μs?

Concept:

Slew rate is the maximum rate of change of output voltage with respect to time.

Slew rate limits the maximum frequency of operation of op-amp

The slew rate is usually measured in volts per microsecond.

Mathematically,

$V_{in} = V_m \sin 2\pi f_m t$ and

$V_0 = AV_{in}$

then, the Slew rate is given as,

$$SR = \left(\frac{dV_0}{dt}\right)_{max} = 2\pi f_{max} V_{0max}$$

∴ We can say that the signal bandwidth f_m is limited by the Slew rate.

Calculation:

Given:

SR = 1 V/μs

V_m = 10V

$$f_{max} = \frac{SR \times 10^6}{2\pi V_M}$$

$$f_{max} = \frac{1 \times 10^6}{2\pi \times 10}$$

f_{max} = 15.92 kHz

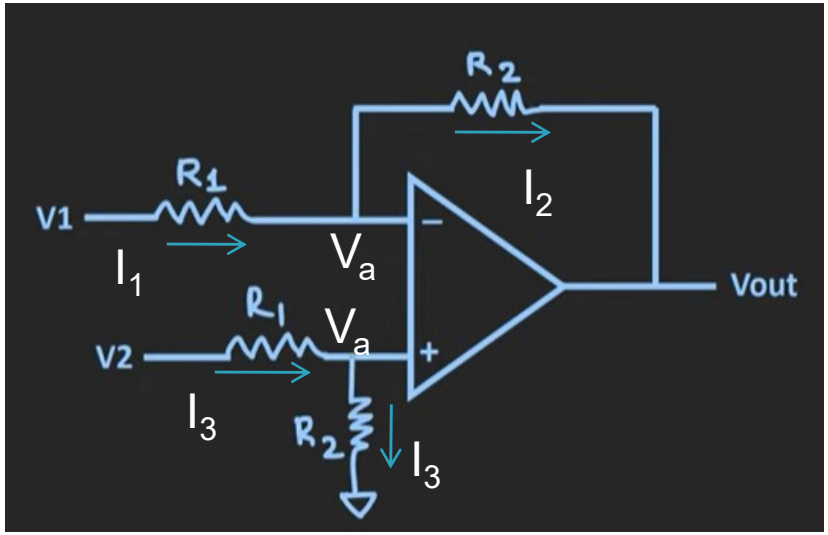
EX.2: Explain importance of slew rate of An op – amp. An op-amp has a slew rate of 1V/μs. What is the maximum frequency of an output sinusoid of peak value 20 V at which the distortion sets in due to the slew rate limitation?

DIFFERENTIAL AMPLIFIER or Subtractor or Difference amplifier:

A subtractor is an electronic circuit that produces an output, which is equal to the difference of the applied inputs.

Differential amplifier will amplify the difference between the two input signals applied at its inverting and non-inverting terminals..

Subtractor is a combination of inverting and non inverting configuration.



Virtual ground concept $V_a = V_b$

At node a

$$V_a = \frac{R_2}{R_2 + R_1} V_2$$

By using Kirchhoff's current law at node b

$I_1 = I_2$

$$\frac{V_1 - V_a}{R_1} = \frac{V_a - V_0}{R_2} \quad \Rightarrow \quad \frac{V_0}{R_2} = \frac{V_a}{R_2} + \frac{V_a}{R_1} - \frac{V_1}{R_1}$$

$$\frac{V_0}{R_2} = V_a\left(\frac{1}{R_2} + \frac{1}{R_1}\right) - \frac{V_1}{R_1}$$

$$\frac{V_0}{R_2} = V_a\left(\frac{R_1+R_2}{R_2R_1}\right) - \frac{V_1}{R_1}$$

Substitute Va in above equation $V_a = \frac{R_2}{R_2 + R_1}V_2$

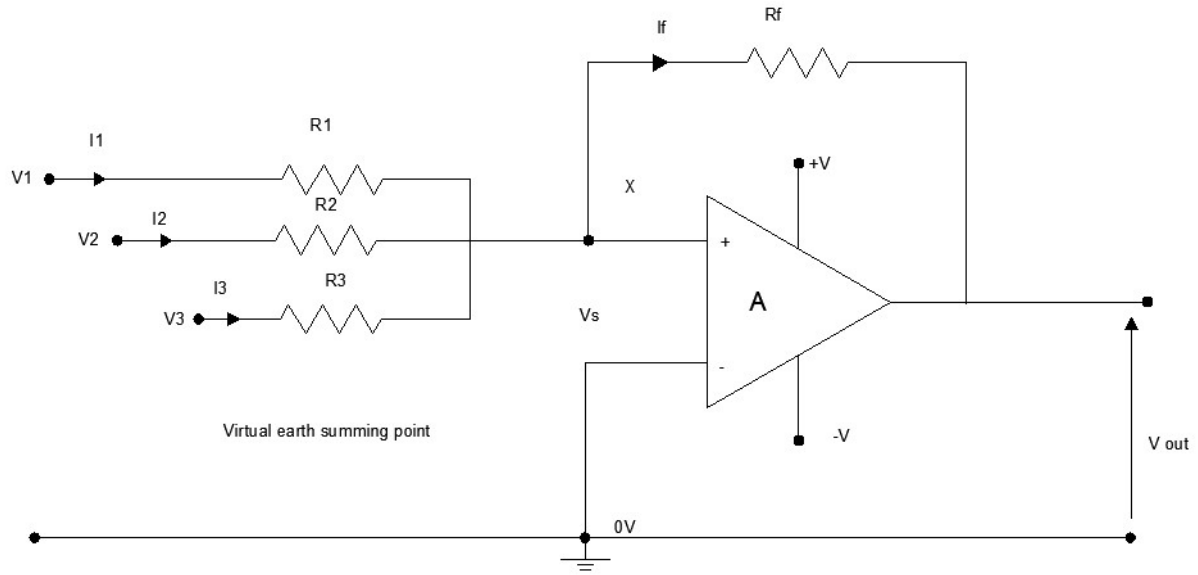
$$\frac{V_0}{R_2} = \frac{R_2}{R_2 + R_1}V_2\left(\frac{R_1+R_2}{R_2R_1}\right) - \frac{V_1}{R_1}$$

$$\frac{V_0}{R_2} = \frac{V_2}{R_1} - \frac{V_1}{R_1} \quad \Rightarrow \quad V_0 = \frac{R_2}{R_1}(V_2 - V_1)$$

Thus, the op-amp based subtractor circuit discussed above will produce an output, which is the difference of two input voltages $V1$ and $V2$.

If can be considered as instrumentation amplifier. But it is not used as an instrumentation amplifier because imbalance may be produced by circuit components.

Adder or Summing amplifier: *The amount of voltage produced at the output of adder is equal to the algebraic sum of input signal voltages.*



According to Kirchhoff's current law at the inverting terminal,

$$i_1 + i_2 + i_3 = i_f$$

$$\frac{V_1 - V_s}{R_1} + \frac{V_2 - V_s}{R_2} + \frac{V_2 - V_s}{R_3} = \frac{V_s - V_0}{R_f}$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_0}{R_f} \text{ (since } V_S = 0)$$

ASSUME: $R_1 = R_2 = R_3 = R_f = R$

$$\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} = -\frac{V_0}{R}$$

Now, commonly take $\frac{1}{R}$ outside.

$$\frac{1}{R}(v1 + v2 + v3) = -\frac{v_0}{R}$$

$$V_0 = -(V_1 + V_2 + V_3)$$

From this, we can understand the output voltage V_o is the sum of input signal voltages called adder.

INSTRUMENTATION AMPLIFIER

INTRODUCTION:

Many industrial systems, process control systems and consumer systems require precise measurement of physical quantities like temperature , pressure, humidity, weight, etc.

For example:

- Sugar factory : flow, level, temperature of juice
- Plastic furnace : Temperature
- Diary plant : Temperature and humidity

- Such physical quantities are converted into proportional electrical signal using transducer.

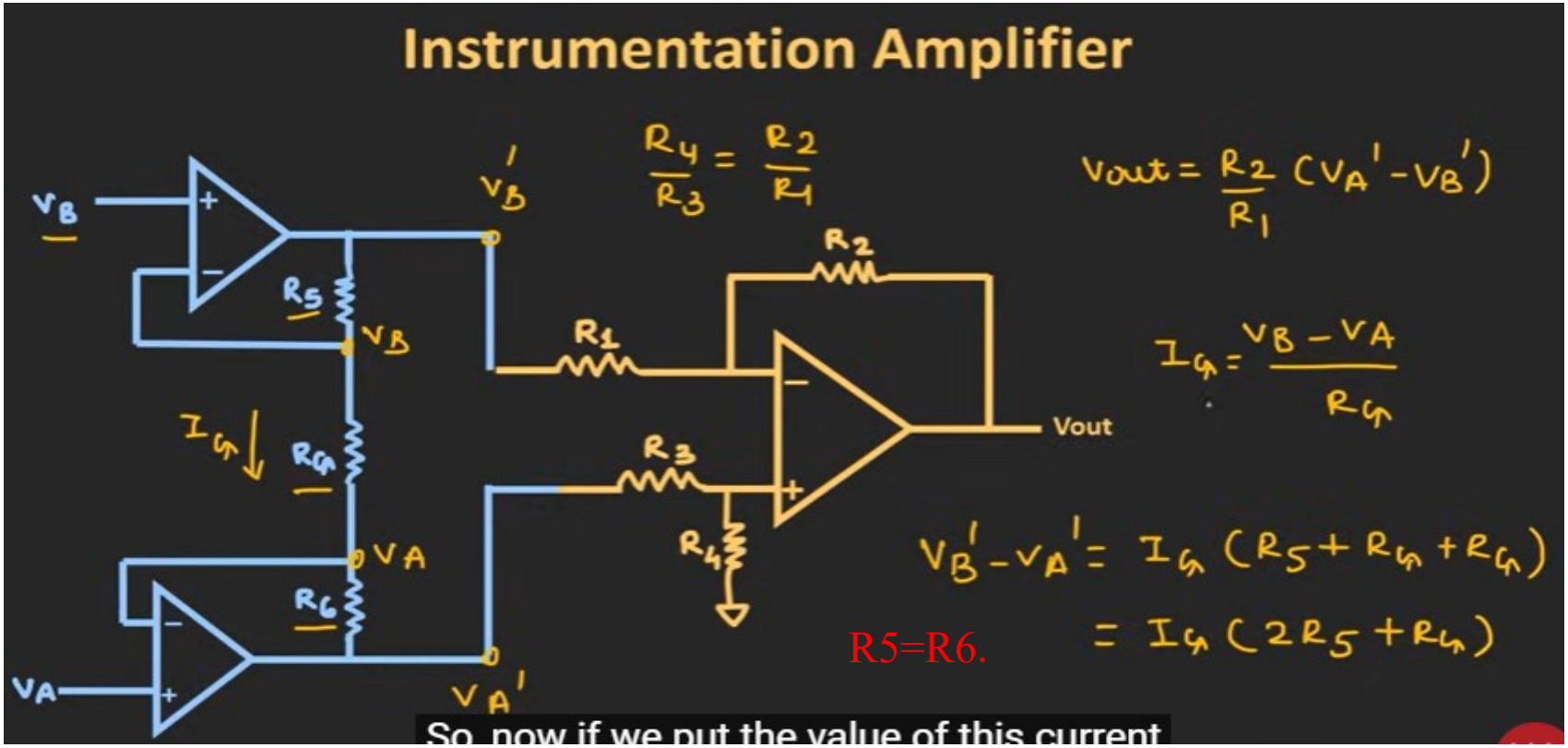
- The most of the transducer outputs are low level signals and not able to drive next stage of system

- Sometimes the transducer is placed far away from control room location and signal may be subjected to noise and atmospheric interference .

An instrumentation amplifier is one kind of differential amplifier, it provides high gain, high CMRR, High input Impedance, High Slew Rate. Most commonly used for Industrial applications to measure temperature, pressure, flow, humidity etc

Definition:

Instrumentation amplifier is basically a high gain difference amplifier with high input impedance that amplifies the low level output signal from transducer by rejecting noise and interference in the signal.



$$V_B' - V_A' = I_G (2R_S + R_G)$$

$$= (V_B - V_A)\left[1 + \frac{2R_S}{R_G}\right]$$

$$V_A' - V_B' = (V_A - V_B)\left[1 + \frac{2R_S}{R_G}\right]$$

$$V_O = \left(\frac{R_2}{R_1}\right)(V_A' - V_B') = \left(\frac{R_2}{R_1}\right)\left(1 + \frac{2R_S}{R_G}\right)(V_A - V_B)$$

INSTRUMENTATION AMPLIFIER:

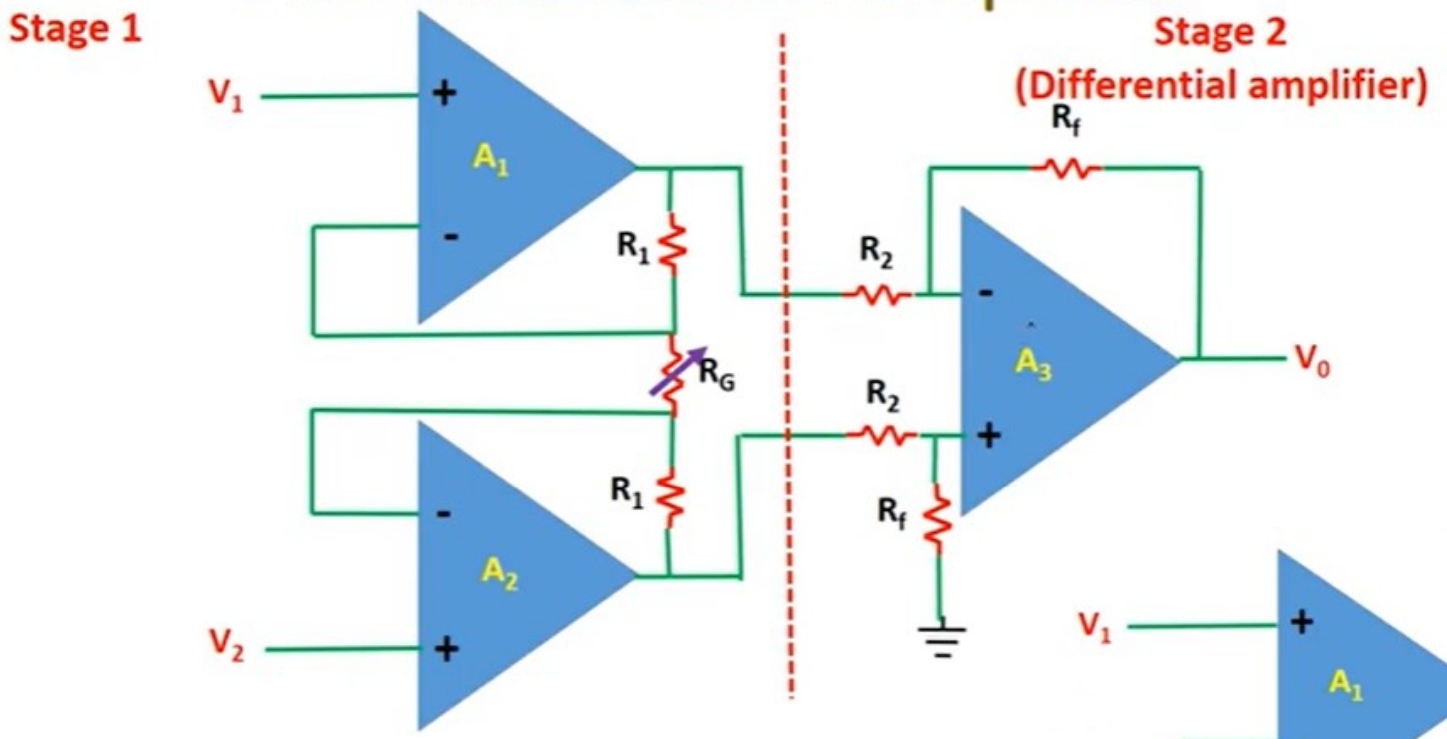
An instrumentation amplifier is a differential op-amp circuit providing high input impedances with ease of gain adjustment through the variation of a single resistor.

An instrumentation (or instrumentational) amplifier is a type of differential amplifier that has been outfitted with input buffer amplifiers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. Instrumentation amplifiers are used where great accuracy and stability of the circuit both short- and long-term are required.

Although the instrumentation amplifier is usually shown schematically identical to a standard operational amplifier (op-amp), the electronic instrumentation amp is almost always internally composed of 3 op-amps. These are arranged so that there is one op-amp to buffer each input (+,−), and one to produce the desired output with adequate impedance matching for the function.

The most commonly used instrumentation amplifier circuit is shown in the figure.

Instrumentation amplifier



Analysis of Stage 1

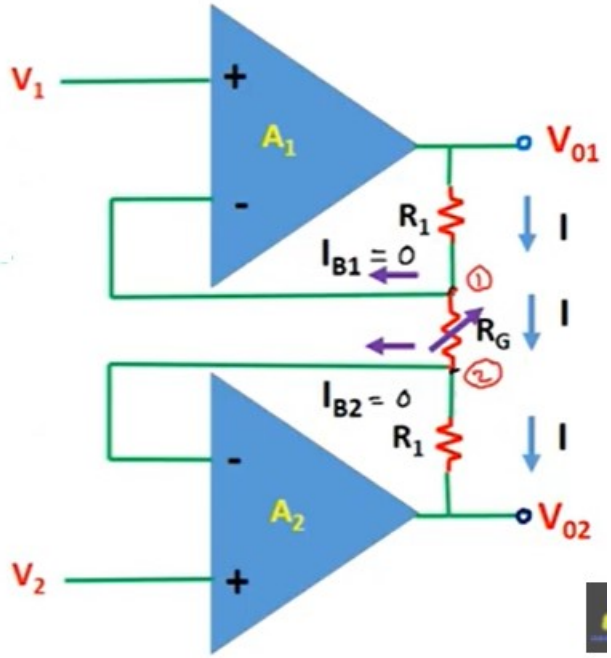
Assuming ideal opamp

The input resistances of all opamps: A_1, A_2, A_3 will be infinite.

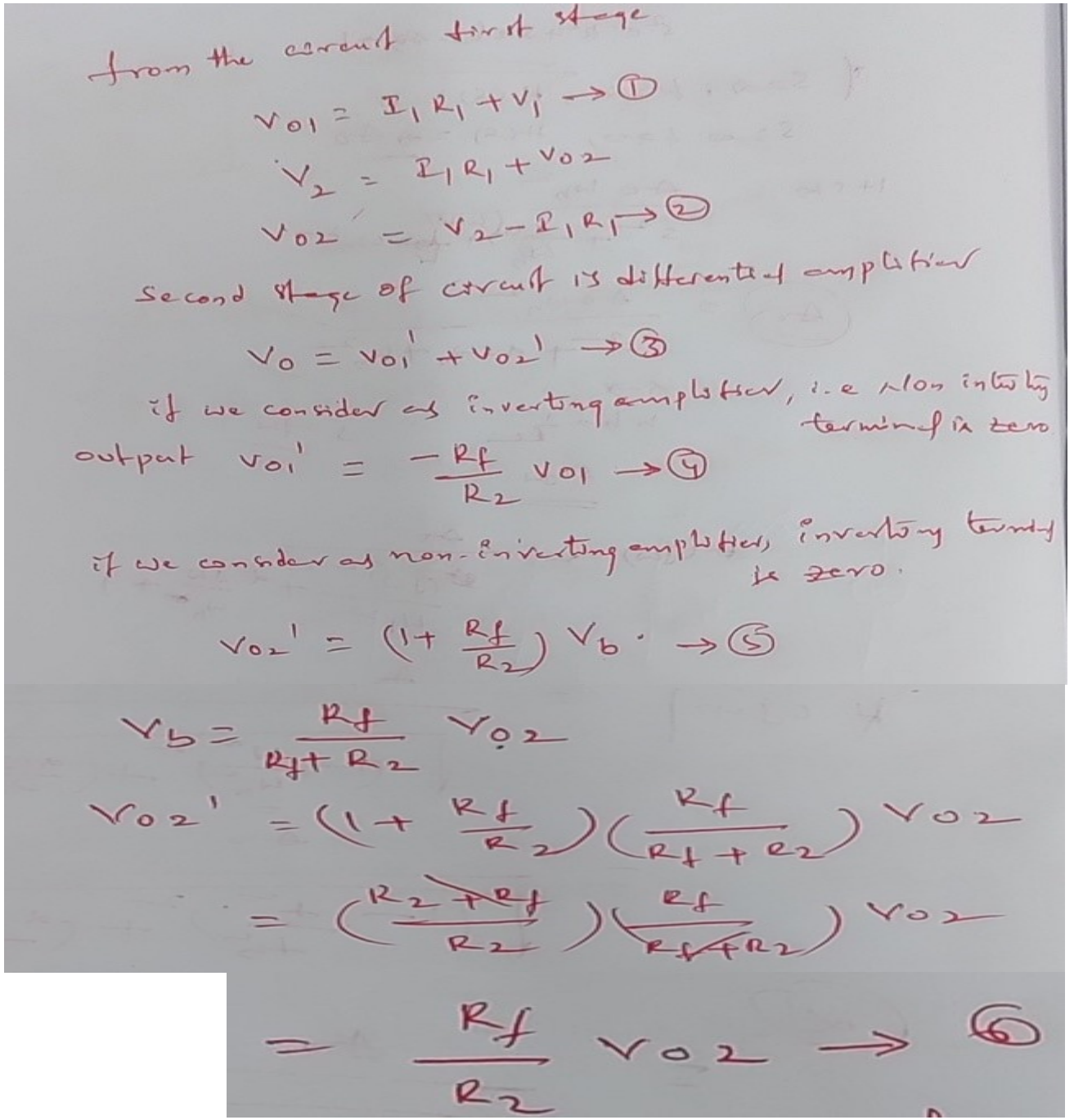
Thus, the input current to all opamps: A_1, A_2, A_3 will be zero. $R_{in} = \infty \Rightarrow I_{in} = 0$

By virtual short circuit concept

Voltage at non inverting terminal = Voltage at inverting terminal



From the circuit



Substitute V_{o1} & V_{o2} in equations (4) & (6)

(4) $\Rightarrow$ $V_{o1}' = \frac{-R_f}{R_2}(I_1 R_1 + V_1) \rightarrow (7)$

(6) $\Rightarrow$ $V_{o2}' = \frac{R_f}{R_2}(V_2 - I_1 R_1) \rightarrow (8)$

(7) & (8) Substitute in equation (3)

$V_o = V_{o1}' + V_{o2}'$

$= \frac{-R_f}{R_2}(I_1 R_1 + V_1) + \frac{R_f}{R_2}(V_2 - I_1 R_1)$

$= \frac{-R_f}{R_2} I_1 R_1 - \frac{R_f}{R_2} V_1 + \frac{R_f}{R_2} V_2 - \frac{R_f}{R_2} I_1 R_1$

$= \frac{R_f}{R_2}(V_2 - V_1) - \frac{2R_f}{R_2} I_1 R_1 \rightarrow (9)$

from the circuit $I_1 = \frac{V_1 - V_2}{R_G} \rightarrow (10)$

(10) in (9)

$V_o = \frac{R_f}{R_2}(V_2 - V_1) - 2\frac{R_f}{R_2}(V_1 - V_2)\frac{R_1}{R_G}$

$= \frac{R_f}{R_2}\left[(V_2 - V_1) - 2(V_1 - V_2)\frac{R_1}{R_G}\right]$

$V_o = \frac{R_f}{R_2}(V_2 - V_1)\left[1 + \frac{2R_1}{R_G}\right]$

Gain

$\frac{V_o}{V_2 - V_1} = \frac{R_f}{R_2}\left(1 + \frac{2R_1}{R_G}\right)$

Overall output voltage

$$V_0 = \frac{R_f}{R_2}\left(1 + \frac{2R_1}{R_G}\right)(V_2 - V_1)$$

Overall gain

$$A_v = \frac{V_0}{(V_2 - V_1)} = \frac{R_f}{R_2}\left(1 + \frac{2R_1}{R_G}\right)$$

Requirements of a Good Instrumentation Amplifier

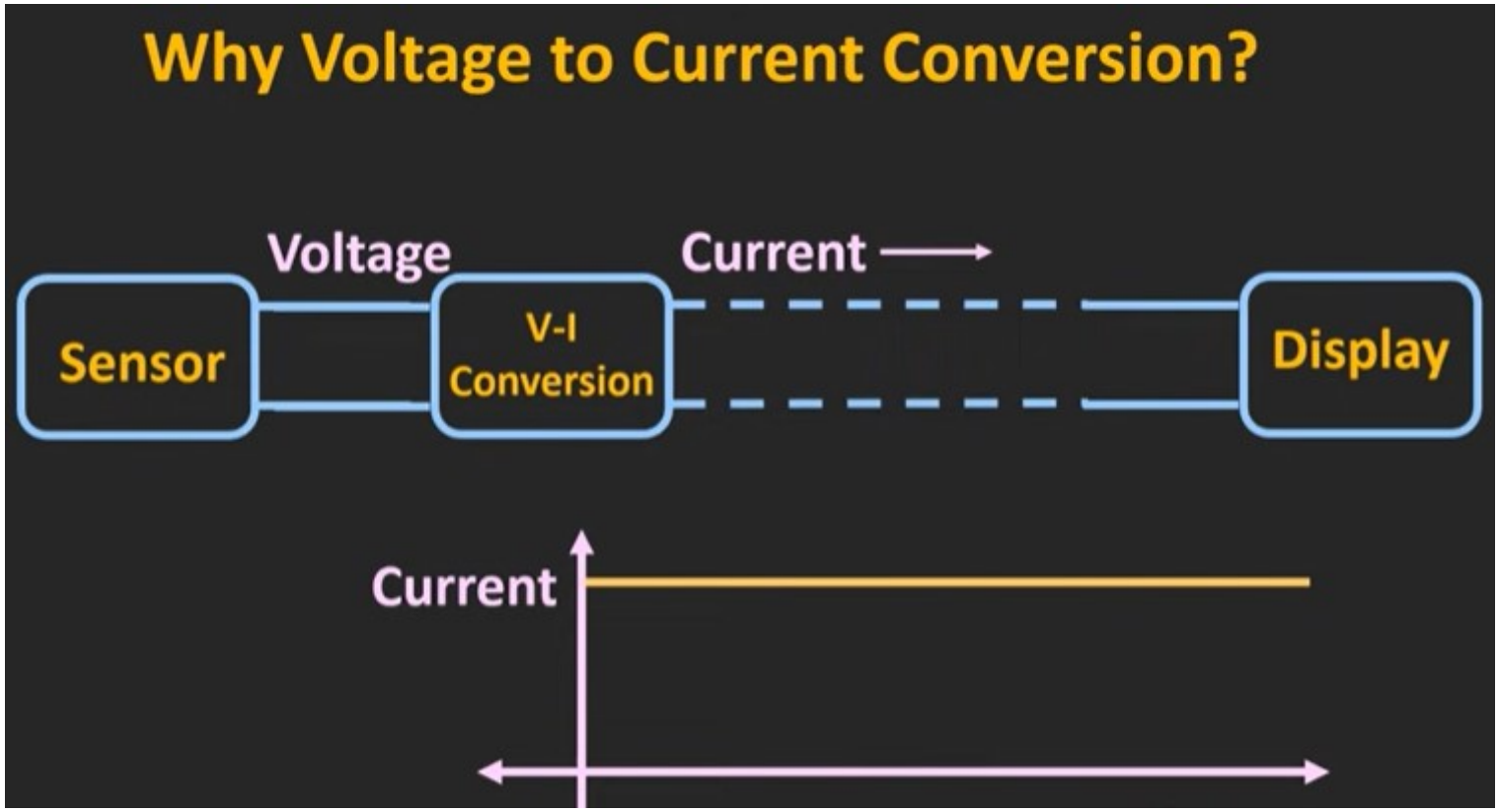
- Finite, Accurate and Stable Gain
- Easier Gain Adjustment
- High Input Impedance:
- Low Output Impedance
- High CMRR
- High Slew Rate

Applications of instrumentation amplifier:

- Temperature controller
- Temperature indicator
- Light intensity meter
- Analog weight scale

Advantages of Three Op-amp Instrumentation Amplifier:

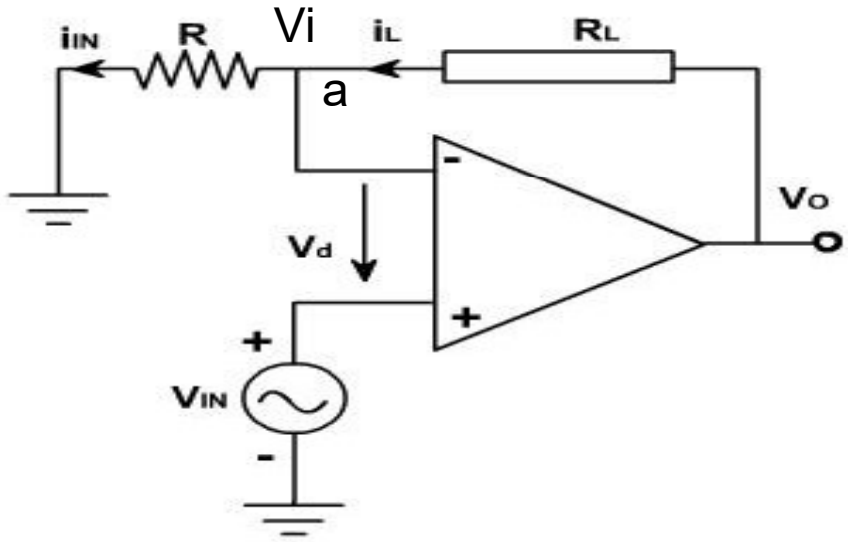
- The gain can be easily varied and controlled by adjusting the value of R_G without changing the circuit structure.
- The gain depends upon the external resistors used. Hence, the gain can be accurately set by choosing the resistor values carefully.
- The input impedance is dependent on the non-inverting amplifier circuits at the input stage. It is very high.
- The output impedance is nothing but the output impedance of the difference amplifier, which is very low.
- The CMRR of the op-amp 3 is very high and almost all of the common mode signal will be rejected.


Why Voltage to Current Conversion?
Voltage
Current
Sensor
V-I
Conversion
Display
Current

VOLTAGE TO CURRENT CONVERTER (Transconductance amplifier)

In voltage to current converter, ***the output current is proportional to input voltage. The voltage to current converter is also called as Transconductance amplifier. There are two types of circuits are possible in voltage to current converter. They are***

i) V to I converter with floating load
ii) V to I converter with grounded load.



The circuit diagram of voltage to current converter with floating load is shown in above figure. The voltage at node 'a' is equal to Vi.

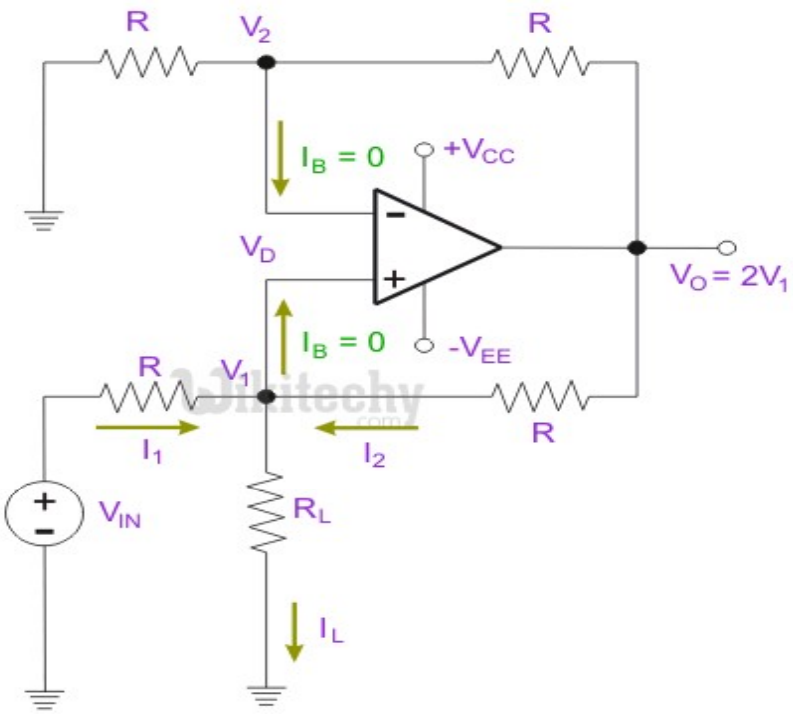
Kcl at node 'a' is $I_i = I_L$

$$\frac{V_i}{R} = I_L$$

$I_L \propto V_i$

Hence, the output (load) current is directly proportional to the input voltage.

A voltage to current converter with grounded load is shown in below figure.



Writing KCL, we get,

$$i_1 + i_2 = i_L$$

$$\frac{V_i - V_1}{R} + \frac{V_0 - V_1}{R} = i_L$$

$$\frac{V_i - V_1 + V_0 - V_1}{R} = i_L$$

$$\frac{V_i - 2V_1 + V_0}{R} = i_L$$

$$V_i + V_0 - 2V_1 = i_L R \qquad \text{----------(1)}$$

Circuit is non inverting amplifier, the output voltage of amplifier is

$$V_0 = (1 + \frac{R_f}{R})(V_1)$$

From the circuit, all resisters are same Rf=R

There fore

$$V_0 = \left(1 + \frac{R}{R}\right)(V_1) = 2V_1$$

Substitute above V0 value in equation (1)

$$V_i + 2V_1 - 2V_1 = I_L R$$

$$V_i = I_L R$$

$$\frac{V_i}{R} = I_L$$

Hence the output load current is directly proportional to the input voltage.

V to I are used to drive the LED connected at load resistor.

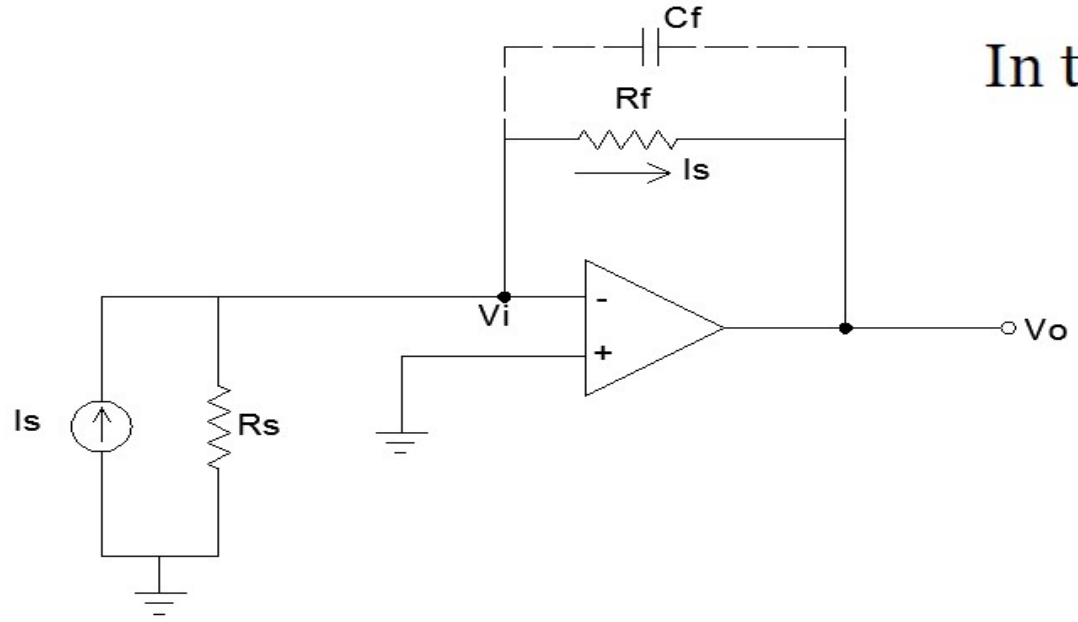
Applications:

Low voltage ac and dc voltmeters
Diode match finders
LED and Zener diode testers

CURRENT TO VOLTAGE CONVERTER: (Transimpedance amplifier)

It produces ***output voltage is proportional to the input current***

The circuit diagram of current to voltage converter is shown in given figure. Since the (-) negative input terminal is at virtual ground, no current flows through Rs and current are flows through the feedback resistor Rf.



$$\text{In this circuit } I_s = \frac{V_i - V_0}{R_f}$$

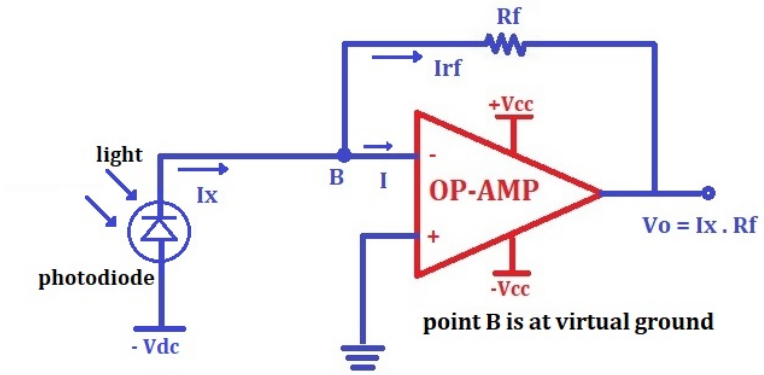
$$V_i = 0$$

$$I_s = \frac{-V_0}{R_f}$$

$$V_0 = -I_s R_f$$

It is also called Transresistance amplifier. The capacitor (Cf) is used to reduce high frequency noise and the possibility of oscillations.

current to voltage converter photodiode:



One of the most important application of I to V converter is as photodetector amplifier to measure the intensity of light as shown in diagram. Also the voltage across the photodiode is kept at 0V due to virtual short.
A photo diode which is reverse biased. Point B i.e. the inverting terminal of the OP-AMP is at virtual ground potential and a negative voltage Vdc is applied at the anode of the photodiode.

When the light is focused on the reverse biased photodiode, a photocurrent starts flowing it is proportional to the intensity of light falling on photodiode as shown. This current acts as the input current to the I-V converter. Hence the output voltage proportional to photocurrent is produced.

Log amplifier: A **logarithmic amplifier**, or a **log amplifier**, is an electronic circuit that produces an output that is proportional to the logarithm of the applied input.

Basics of Logarithmic Amplifier

- By logarithmic Rules, we can convert multiplication into Addition and division into subtraction.

$$\text{Log}\,(A \times B) = \text{Log}\,(A) + \text{Log}\,(B)$$

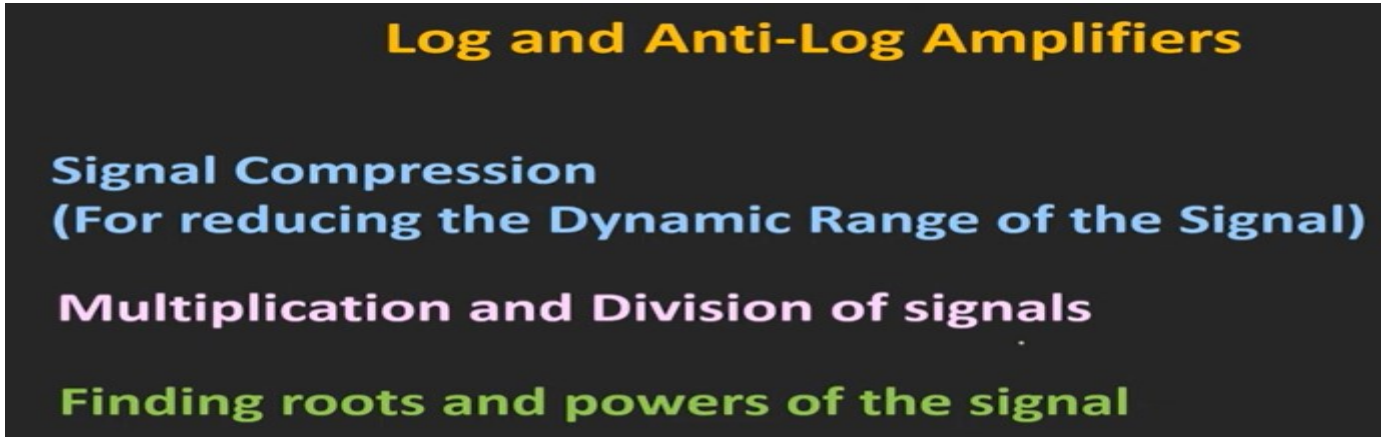
$$\text{Log}\,(A/B) = \text{Log}\,(A) - \text{Log}\,(B)$$

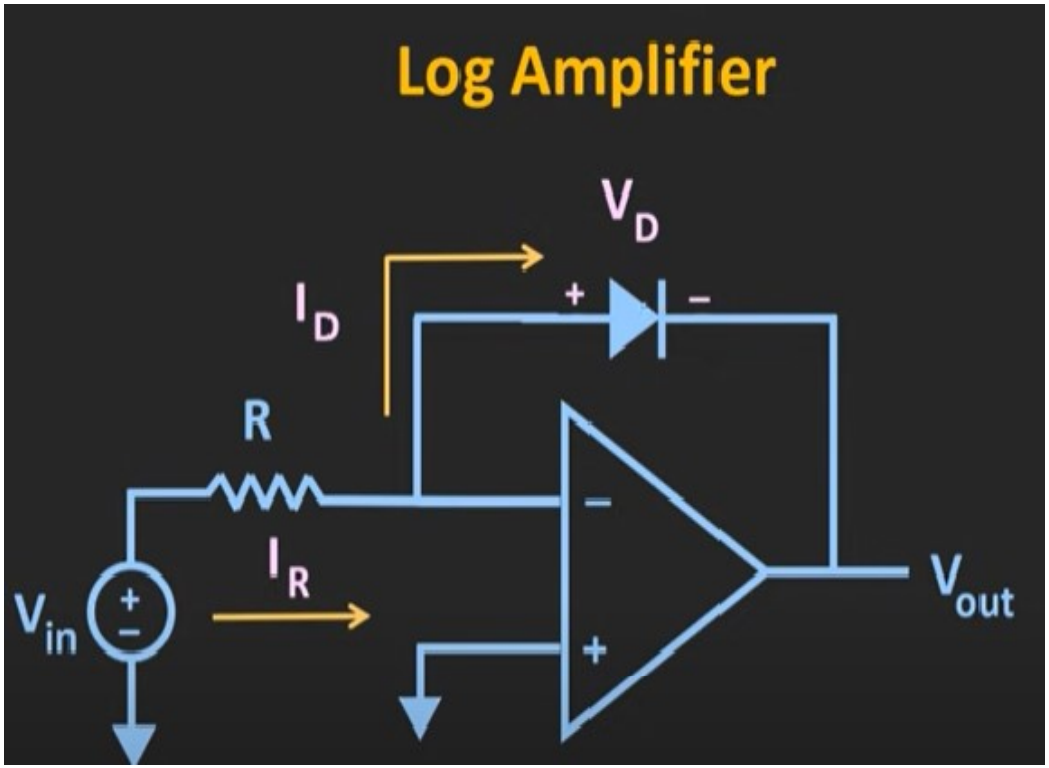
- By logarithmic Rules, we can convert Power into Multiplication.

$$\text{Log}\,(A^B) = B \times \text{Log}\,(A)$$

- So, logarithmic properties are used to simplify mathematics.

$$V_{OUT} \propto \log\,(V_{IN})$$





Current passing through Diode I_D

$$I_D = I_S \left(e^{\left(\frac{V_d}{\eta V_T}\right)} - 1 \right)$$

I_S - Reverse Saturation Current

V_T - Thermal Voltage

V_d - Forward Voltage of diode

η - Ideality Factor (1-2)

$e^{\left(\frac{V_D}{\eta V_T}\right)}$ > 1 then I_D is

$$I_D \simeq I_S \times e^{\left(\frac{V_D}{\eta V_T}\right)}$$

$$V_T = \frac{kT}{q}$$

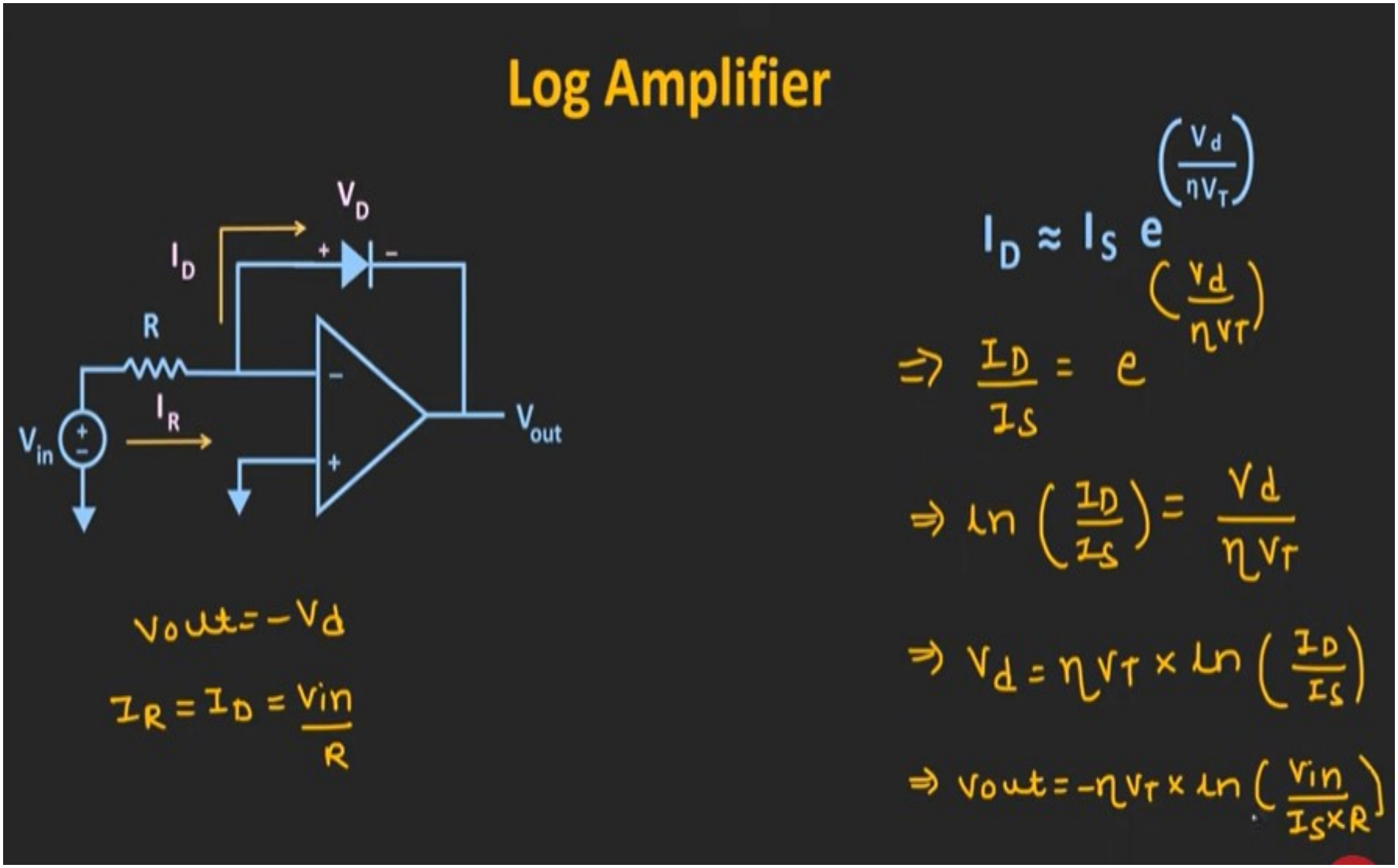
k - Boltzmann Constant (1.38×10^{-23} Joules/Kelvin)

T - Temperature of the Diode

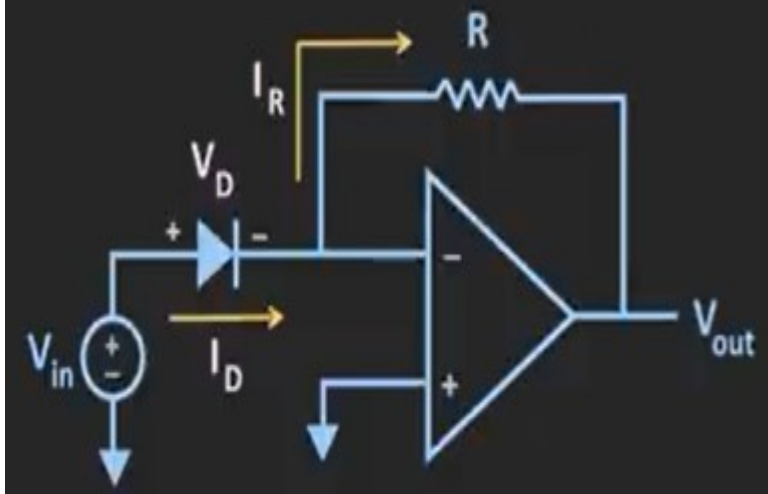
q - Charge of electron (1.6×10^{-19} Coulombs)

At 300 K, $V_T \approx 25.8$ mV

Log amplifier: A **logarithmic amplifier**, or a **log amplifier**, is an electronic circuit that produces an output that is proportional to the logarithm of the applied input.



Anti-Log Amplifier



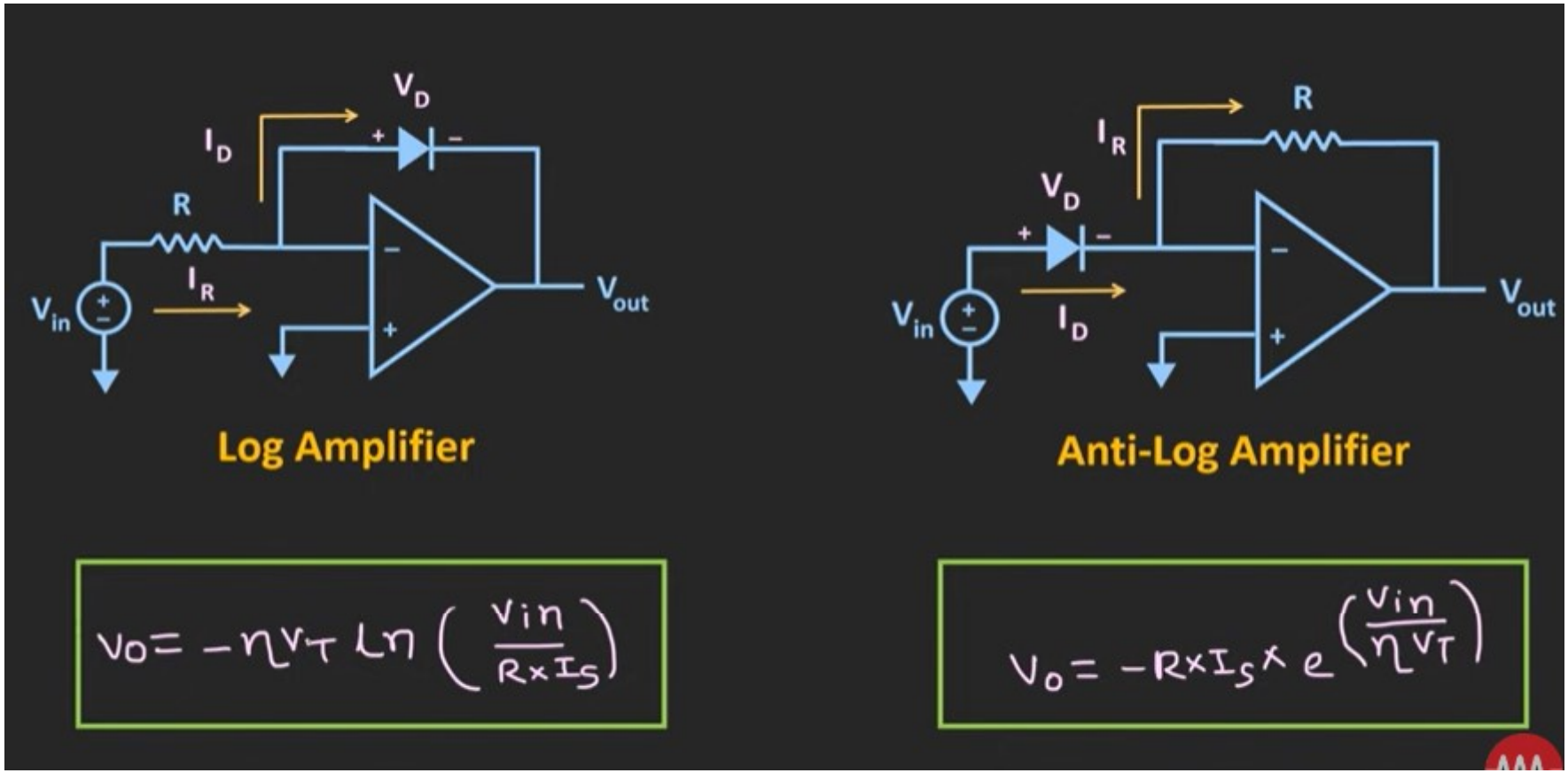
$$I_D \simeq I_S \times e^{\left(\frac{V_D}{\eta V_T}\right)}$$

$$V_{out} = -R \times I_D$$

$$= -R \times I_S \times e^{\left(\frac{V_D}{\eta V_T}\right)}$$

$$V_{out} = -R \times I_S \times e^{\left(\frac{V_{in}}{\eta V_T}\right)}$$

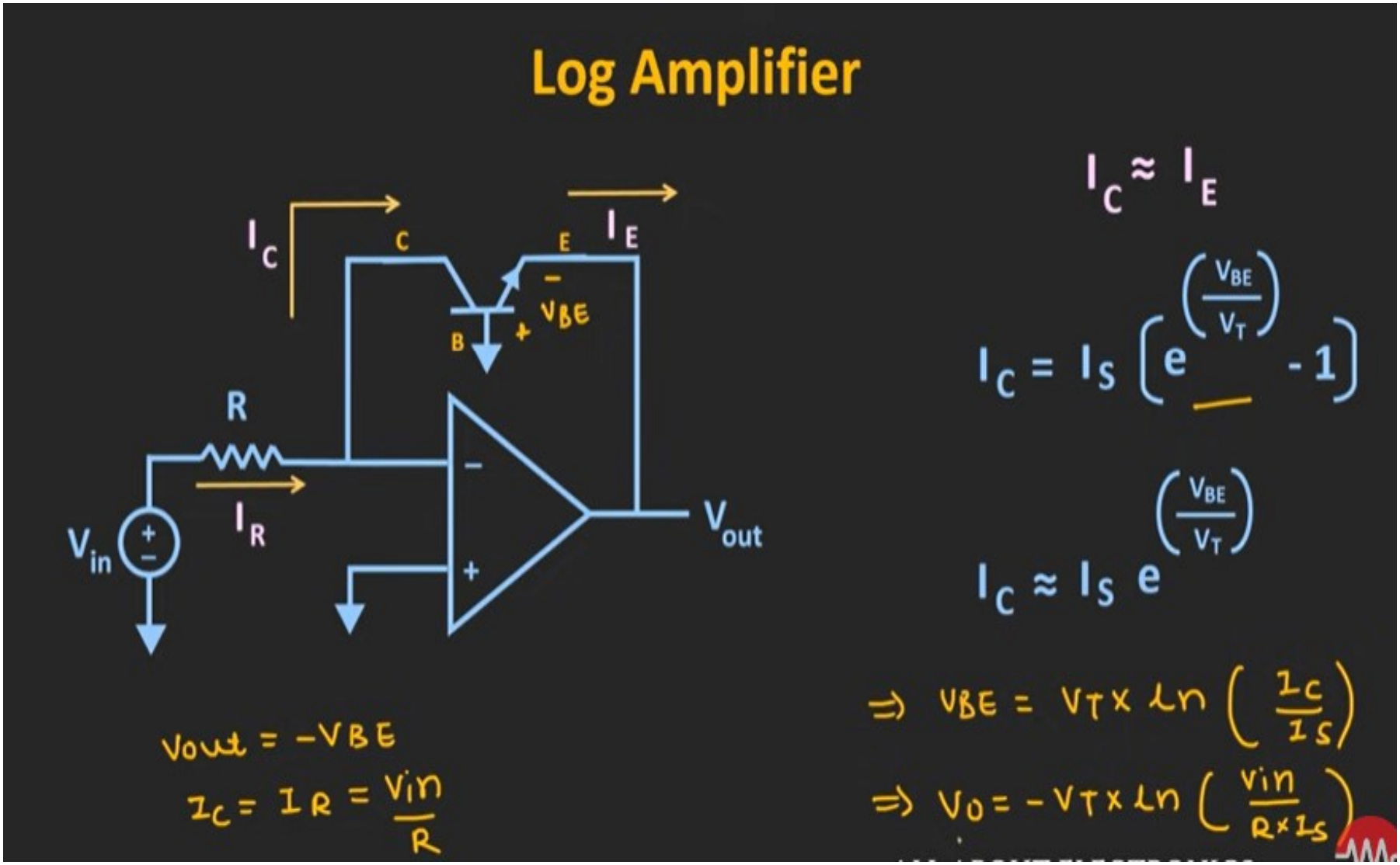
$V_{in} = V_D$



The output voltage also depends upon Ideality factor, reverse saturation current and thermal voltage. Thermal voltage and reverse saturation currents varies with temperature.

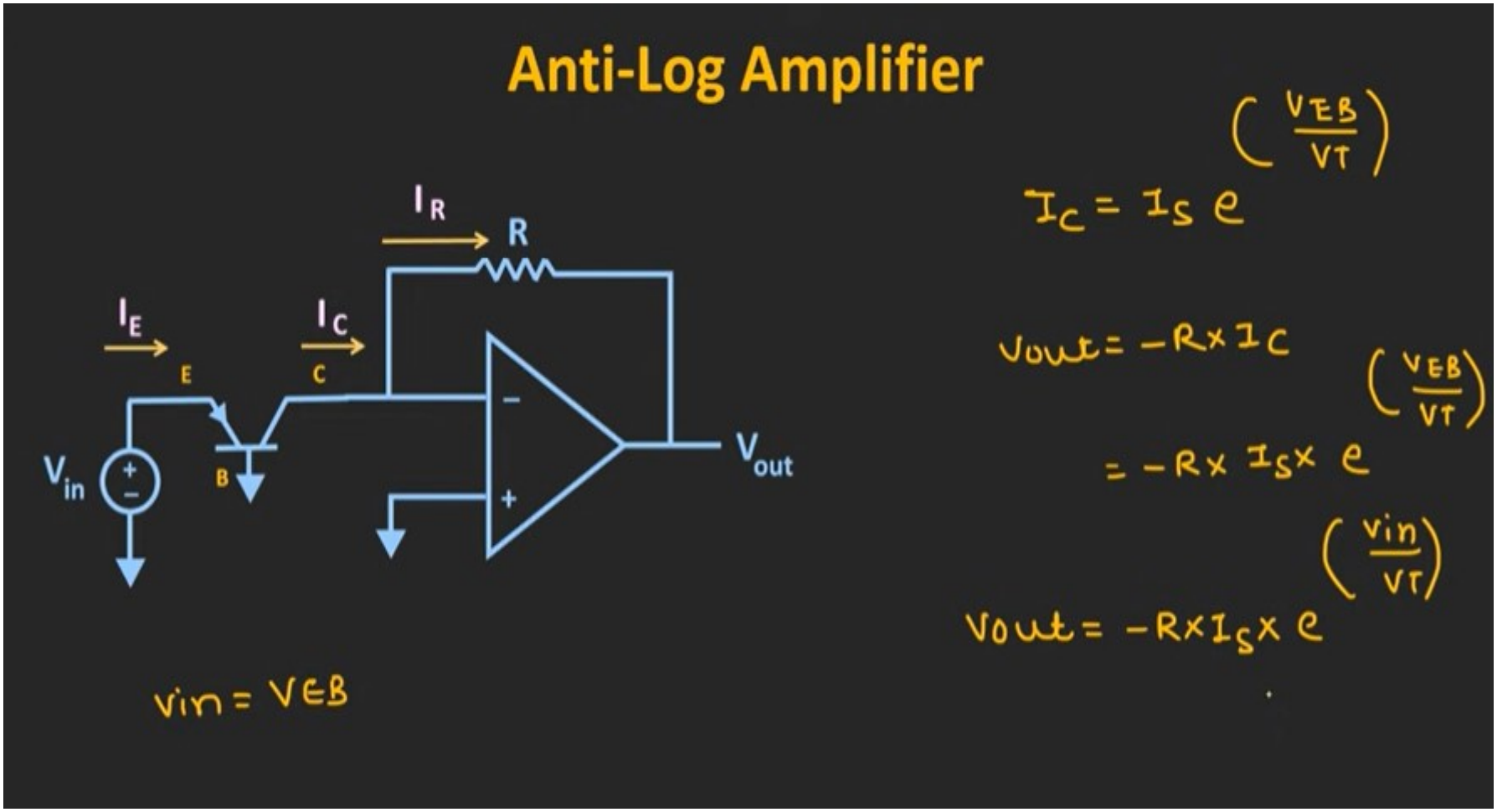
The range of Ideality factor is 1-2. Because of this Ideality factor, the dynamic range of circuit used to get reduced. This limitation will be overcome by replacing diode by transistor to improve the dynamic range of circuit. Log and anti log amplifiers designed by using transistor as discussed below.

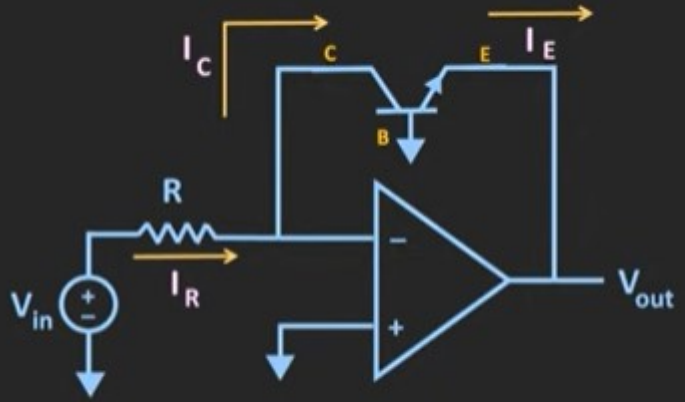
Log amplifier: A **logarithmic amplifier**, or a **log amplifier**, is an electronic circuit that produces an output that is proportional to the logarithm of the applied input.



Anti-Logarithmic Amplifier

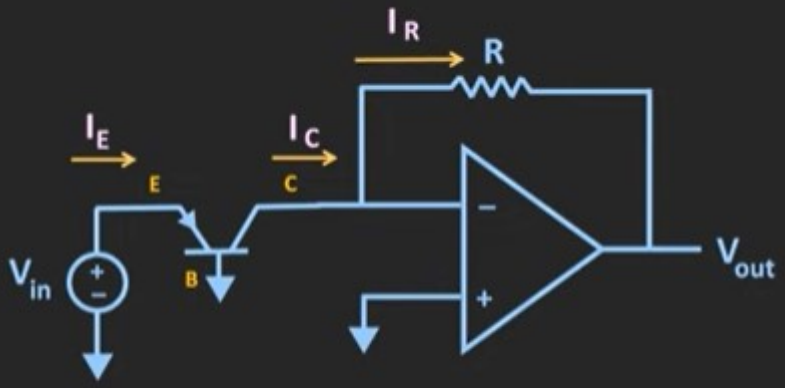
An **anti-logarithmic amplifier**, or an **anti-log amplifier**, is an electronic circuit that produces an output that is proportional to the anti-logarithm of the applied input.





Log Amplifier

$$V_o = -V_T \ln\left(\frac{V_{in}}{I_S \times R}\right)$$

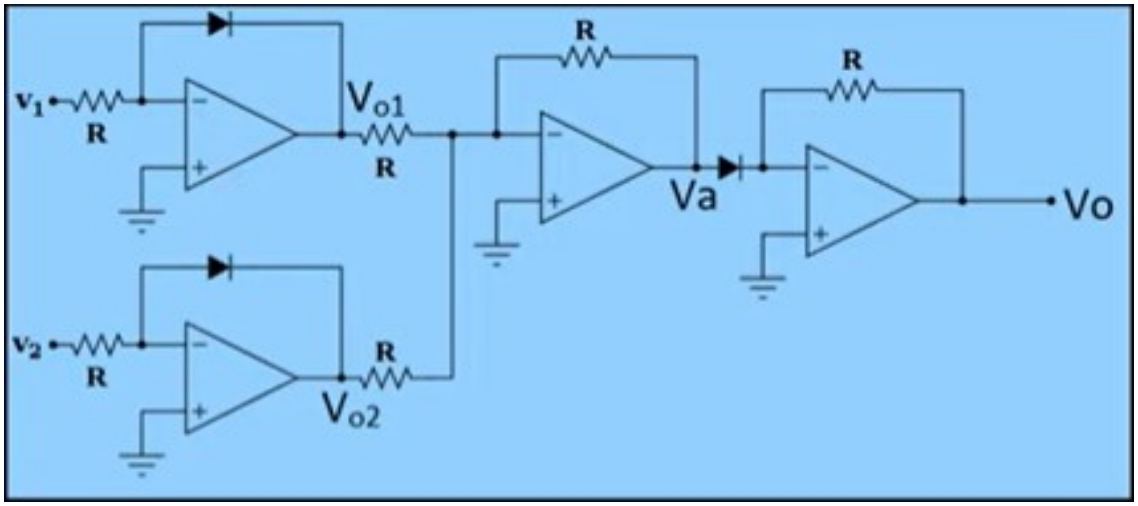


Anti-Log Amplifier

$$V_o = -R \times I_S \times e^{\left(\frac{V_{in}}{V_T}\right)}$$

Analog multiplier:

An analog multiplier is a device that produces an output voltage or current that is proportional to the product of two or more independent input voltage or current. The analog multiplier is designed using log and antilog amplifier. A log amplifier can be constructed using a diode r transistors in the feedback to the opamp. The output of log amplifier is dependent on the saturation current which varies from transistor to transistor and also with temperature. Antilogarithmic or exponential amplifier does the exact opposite operation of a log amplifier. In analog amplifier the two inputs are given in the form of voltages to log amplifier respectively. The output voltage from the log amplifier are added and inverted by the unity gain summing amplifier. Output of summing amplifier is given to the antilog amplifier. The output at antilog amplifier is the multiplication of two inputs but it is in inverted form. So we are using an inverting amplifier to get the desired output. The final output is V0 = kV1*V2.



- For Log amplifier :$V_o = -\eta V_T \log \frac{V_{in}}{I_0 R}$
- $V_{o1} = -\eta V_T \log \frac{V_1}{I_0 R}$
- $V_{o2} = -\eta V_T \log \frac{V_2}{I_0 R}$
- **$V_a = -(V_{o1}+V_{o2})$**
- $= -\left(-\eta V_T \log \frac{V_1}{I_0 R} - \eta V_T \log \frac{V_2}{I_0 R}\right)$

$$V_a = \eta V_T \left(\log \frac{V_1}{I_0 R} + \log \frac{V_2}{I_0 R}\right)$$

$$V_a = \eta V_T \log \frac{V_1 \cdot V_2}{I_0^2 R^2} \quad \text{—①}$$

$$V_0 = -I_0 R \text{ antilog } \frac{\eta V_T \log \frac{V_1 V_2}{I_0^2 R^2}}{\eta V_T} = -I_0 R \frac{V_1 V_2}{I_0^2 R^2} = -\frac{V_1 V_2}{I_0 R}$$

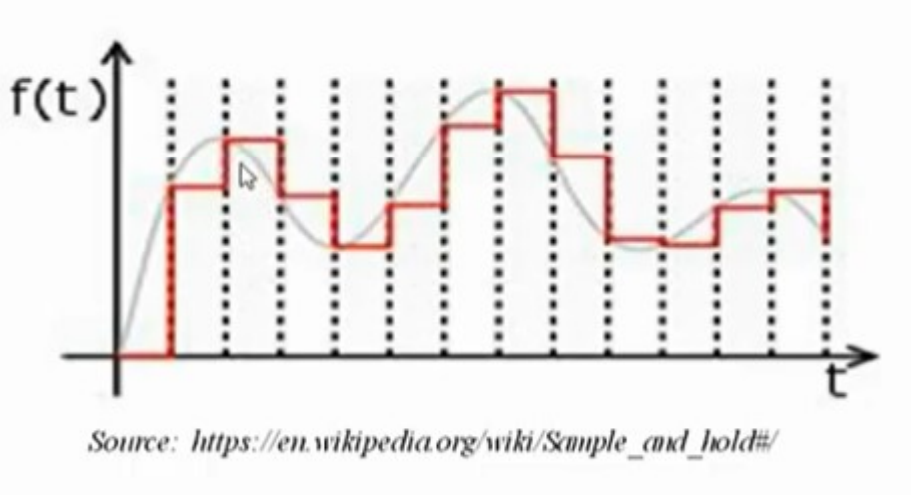
$$V_0 = -k V_1 V_2 \left\{ k = \frac{1}{I_0 R} \right.$$

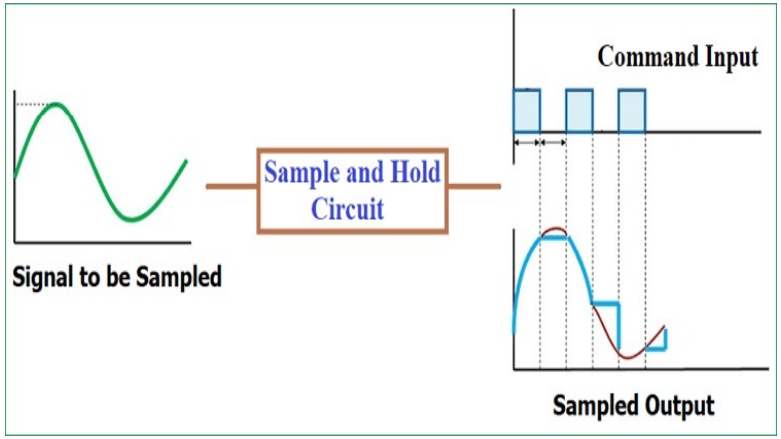
V0 α V1 V2

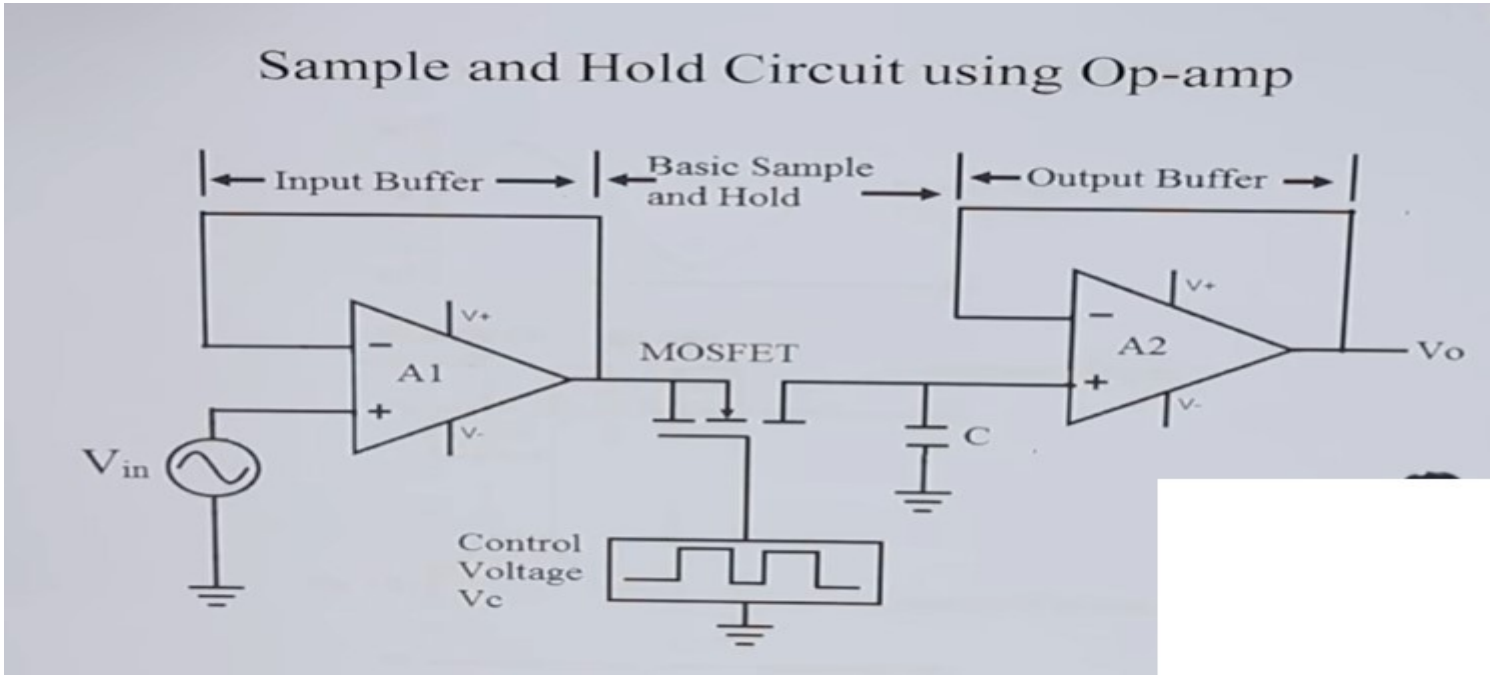
Sample and Hold Circuit:

Samples the input signal and holds the sampled value for specific time period i.e until input is sampled again.

The time during which sample and hold circuit generates the sample of the input signal is called **sampling time.** Similarly, the time duration of the circuit during which it holds the sampled value is called **holding time.**







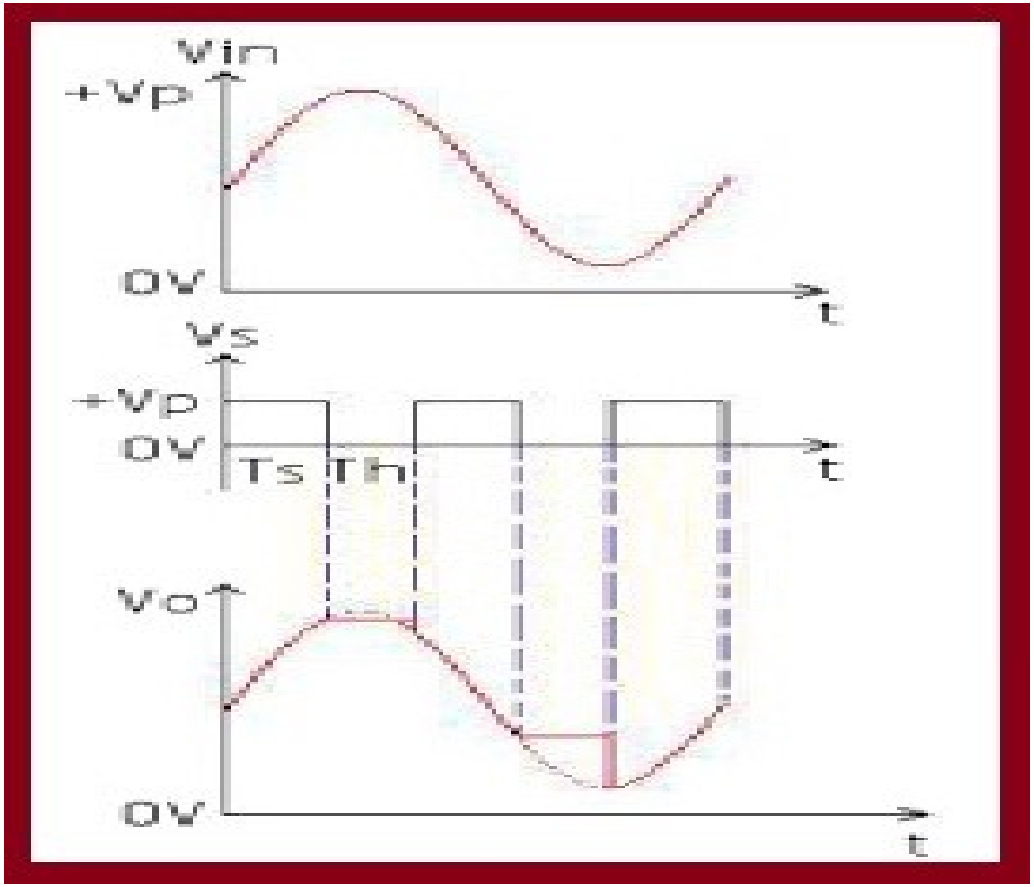
A1 buffer amplifier avoids loading of input source, A2 avoids loading of capacitor.

When the MOSFET works as a closed switch, the analog signal given to it through the drain terminal will be fed to the capacitor. Then the capacitor will charge to its peak value. When the switch is released, then the capacitor discontinues charging. Due to the high impedance op-amp connected at the circuit end, the capacitor will knowledge high impedance due to this it cannot get discharged.

This directs to the holding of the charge by the capacitor for the exact amount of time. This can be referred as holding period. And the time in which samples of i/p voltage is produced is named sampling period. The o/p processed by op-amp throughout the holding period. So, holding period holds implication for Op-Amps.

Applications

- Analog to digital converters
- Pulse width modulation
- Digital interfacing
- Sampling Oscilloscopes
- Data Distribution System
- Digital Voltmeters
- Analog Signal Processing
- Signal Constructional Filters
- Data Conversion System



Rectifiers

An electronic circuit, which produces either DC signal or a pulsated DC signal, when an AC signal is applied to it is called as a **rectifier**. Conventional rectifier is not rectify the AC voltage below 0.7V.

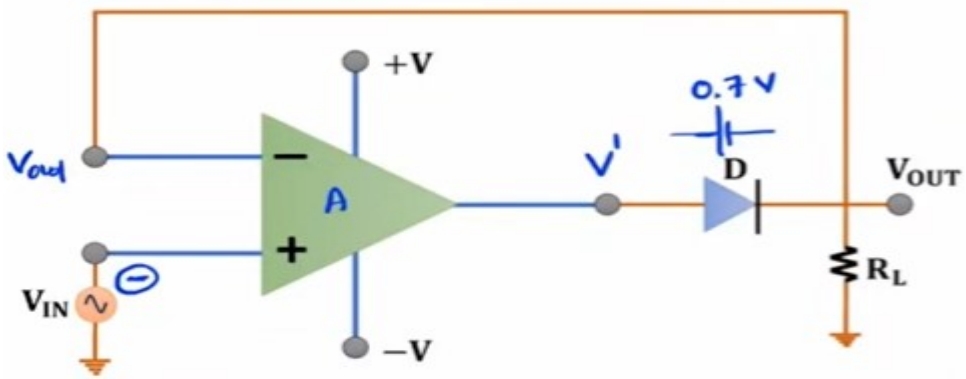
The precision rectifier makes it possible to rectify voltages of small magnitude(i.e below0.7)

The rectifier circuit used for circuit detection with op-amp is called precision rectifier.

Basics of Precision Rectifier

- In a typical rectifier circuit, we use diodes to rectify the AC signal into the DC signal. This rectification method can only be used if the input voltage to the circuit is greater than the CUT-IN or KNEE voltage of the diode (0.7V for Si).
- So, if the input signal ranges in a few millivolts, then a normal rectifier can not rectify it.
- To overcome this issue, the precision rectifier is used to rectify signals in order of a few millivolts.

Half wave Precision Rectifier using Operational Amplifier



- OpAmp is connected in voltage follower configuration.
- Diode is used to clip the negative cycle of OpAmp.
- Here a combination of OpAmp + Diode is acting like a Super Diode.
- In the negative half cycle, Diode stays in reverse bias.
- In the negative half cycle, OpAmp out goes in negative saturation, So the given circuit has limitations with higher frequency operations.

∴ Output of OpAmp

$\Rightarrow V' = A(V_{in} - V_{out})$

$\Rightarrow 0.7 + V_{out} = A(V_{in} - V_{out})$

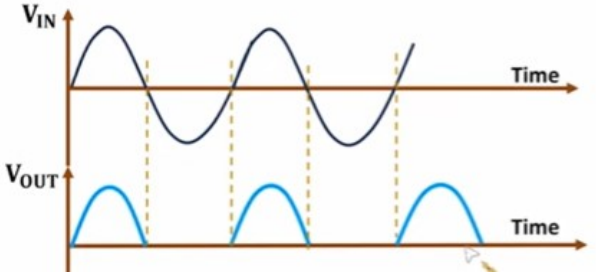
$\Rightarrow \frac{0.7 + V_{out}}{A} = V_{in} - V_{out}$

$\Rightarrow 0 = V_{in} - V_{out}$

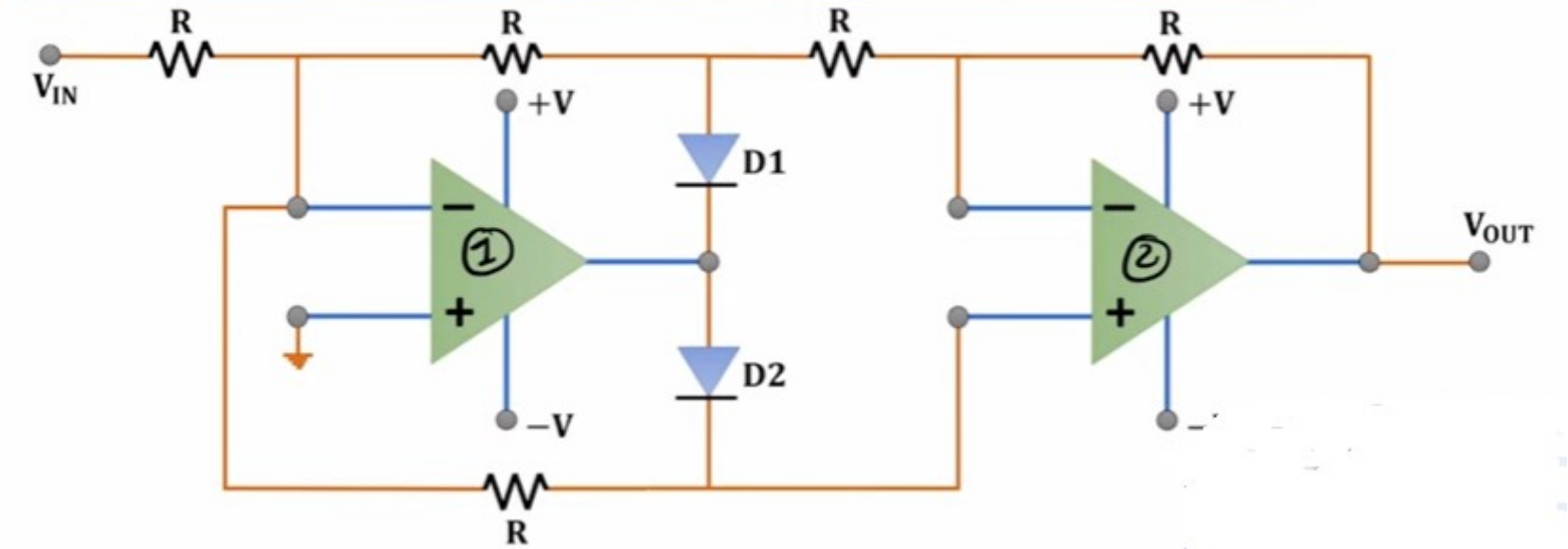
$\Rightarrow V_{in} = V_{out}$

Gain A is very large i.e. 10^5

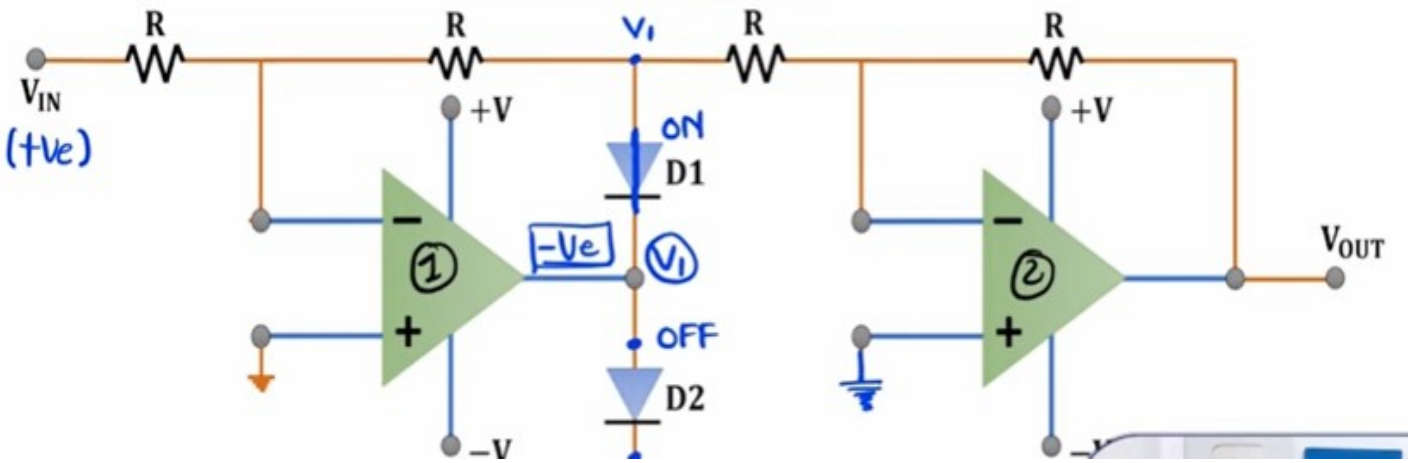
$(0.7+V0) / A = 0$



Full wave Precision Rectifier using Operational Amplifier



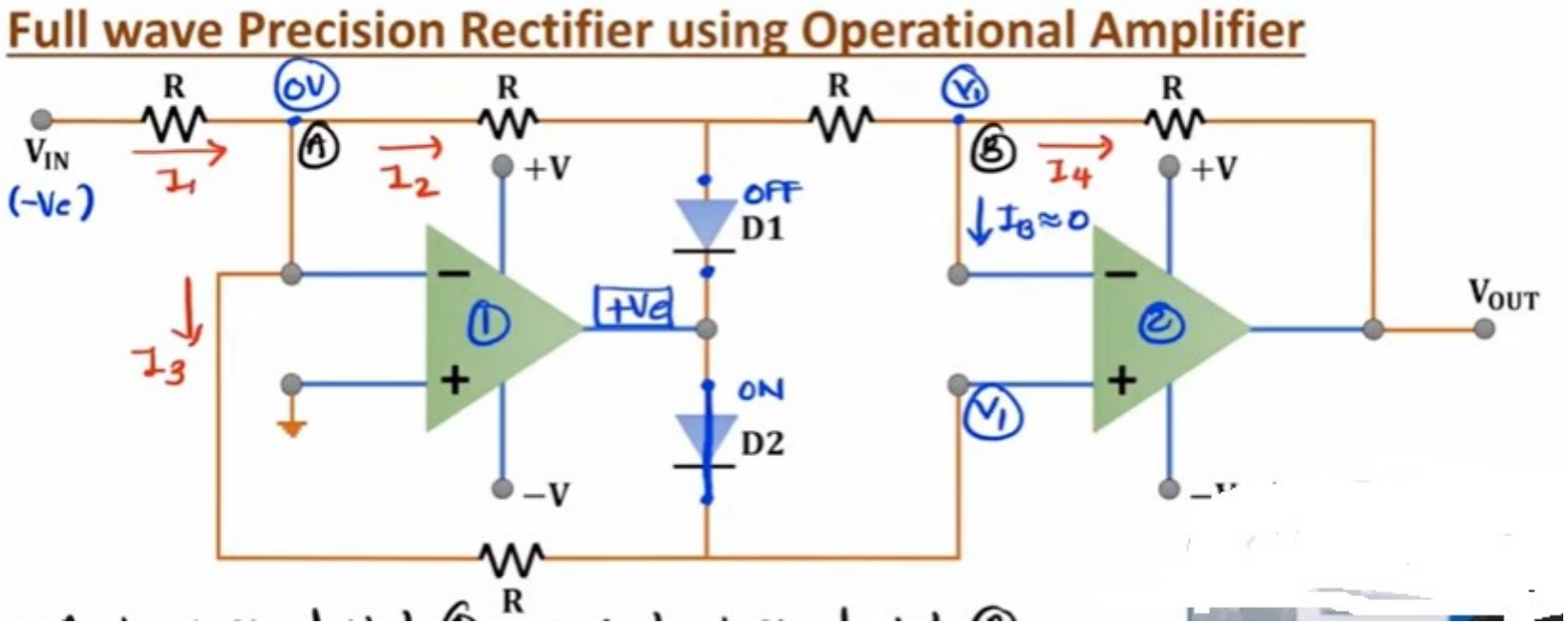
Input is positive Vi = + ve



$\therefore V_1 = V_{in}\left(-\frac{R}{R}\right) = -V_{in}$

$V_{out} = V_1\left(-\frac{R}{R}\right) = -V_1 = -(-V_{in}) = V_{in}$

Full wave Precision Rectifier using Operational Amplifier



Input is negative Vi= -Ve

⇝ Apply KCL at Node (A)

$\Rightarrow I_1 = I_2 + I_3$

$\Rightarrow \frac{V_{in}}{R} = -\frac{V_1}{2R} - \frac{V_1}{R}$

$\Rightarrow V_{in} = -\frac{3}{2}V_1$

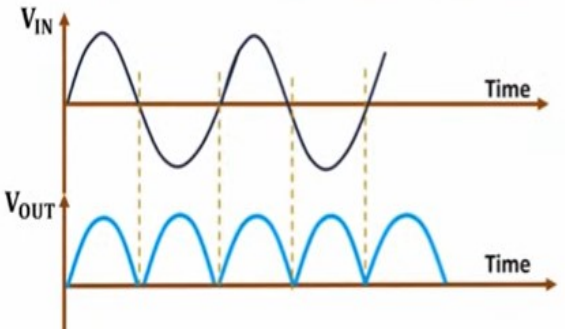
⇝ Apply KCL at Node (B)

$\Rightarrow I_2 = I_4$

$\Rightarrow -\frac{V_1}{2R} = \frac{V_1 - V_{out}}{R}$

$\Rightarrow -\frac{V_1}{2} - V_1 = -\frac{3V_1}{2} = -V_{out}$

$\rightarrow V_{in} = -V_{out}$



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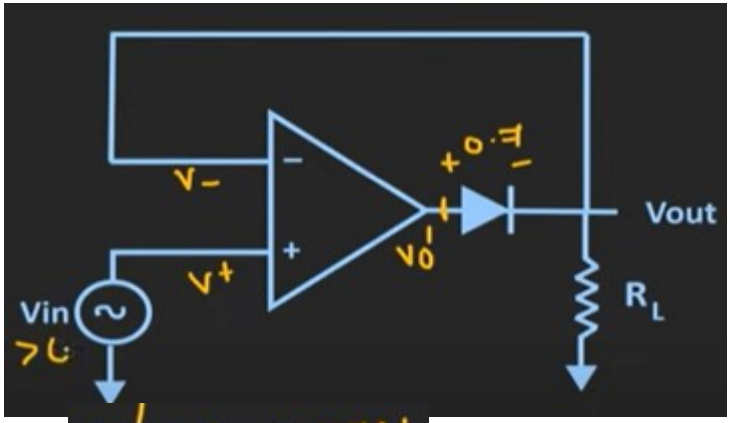
The rectifier circuit used for circuit detection with op-amp is called precision rectifier.

Precision Rectifier



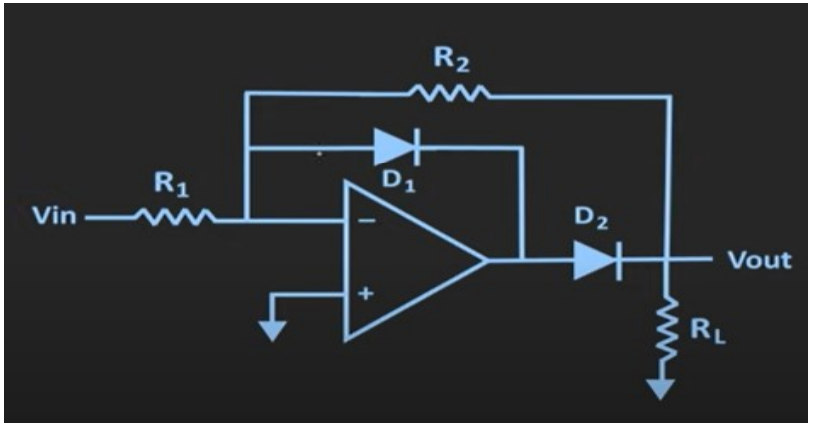
$V_0' = V_0 + 0.7V$

$V_0' = A_{OL} \times (V^+ - V^-)$

$\Rightarrow \frac{V_0 + 0.7V}{A_{OL}} \simeq 0 = V^+ - V^-$

$\Rightarrow V^+ = V^- \Rightarrow V_{out} = V_{in}$

Modified Precision Rectifier



If $V_{in} > 0$, D1 conducts, it is inverting amp so o/p of amp is –ve, D2 is reverse bias (open), output V0=0

If $V_{in} < 0$, D1 is off, D2 is on, output V0= -(R2/R1)Vi

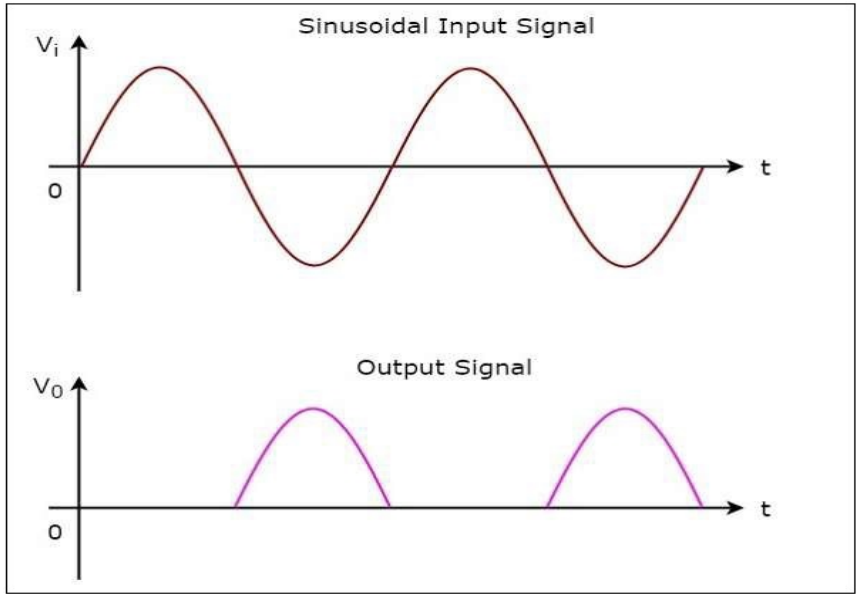
For the **negative half cycle** of sinusoidal input, the output of the op-amp will be positive. Hence, the diodes D_1 will be reverse biased and D2 will be forward biased respectively.

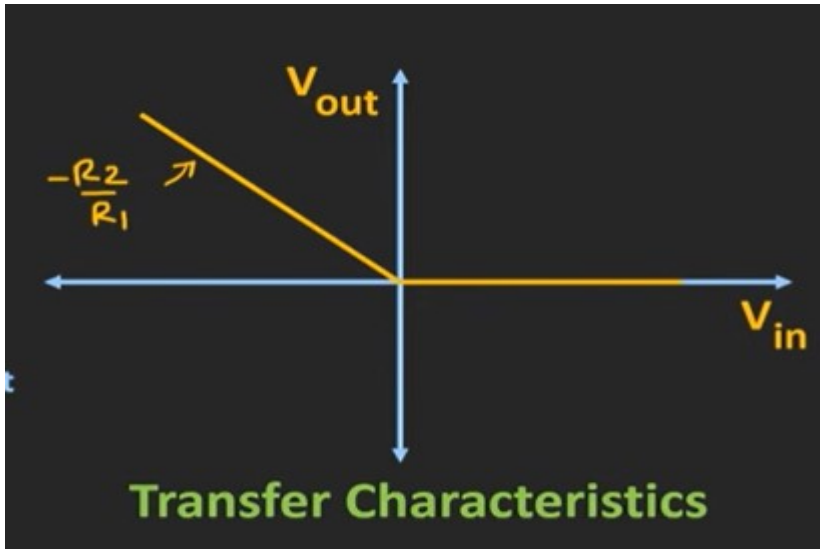
For the **positive half cycle** of the sinusoidal input, the output of the op-amp will be negative. Hence, diode D_1 will be forward biased.

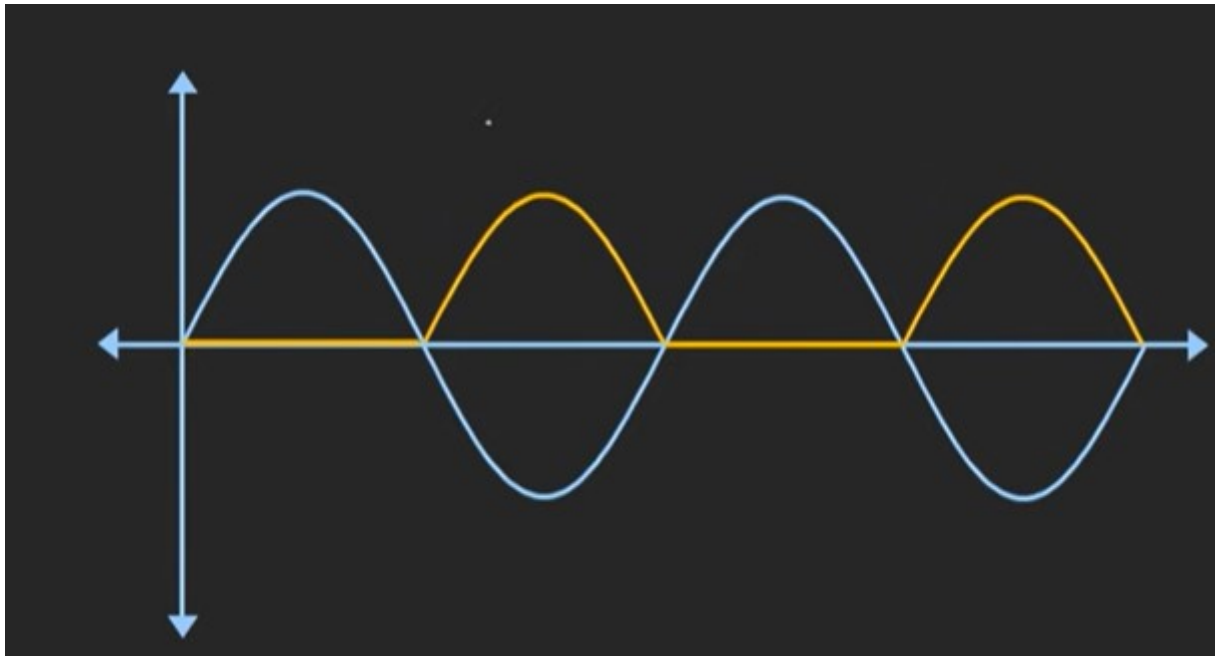
When diode D_1 is in forward bias, output voltage of the op-amp will be -0.7 V. So, diode D_2 will be reverse biased. Hence, the **output voltage** of the above circuit is **zero** volts. Therefore, there is **no (zero) output** of half wave rectifier for the positive half cycle of a sinusoidal input.

For the **negative half cycle** of sinusoidal input, the output of the op-amp will be positive. Hence, the diodes D_1 and D_2 will be reverse biased and forward biased respectively. So, the output voltage of above circuit will be −

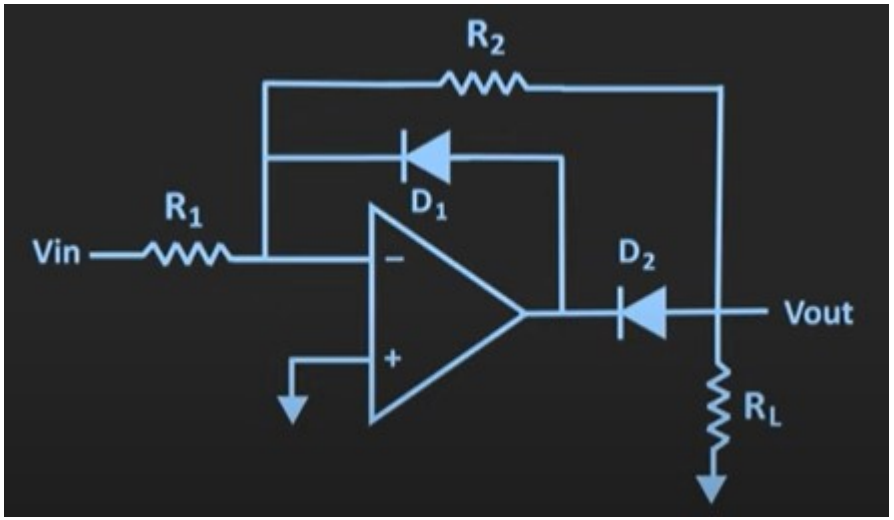
$$V_0 = -\left(\frac{R_f}{R_1}\right) V_1$$

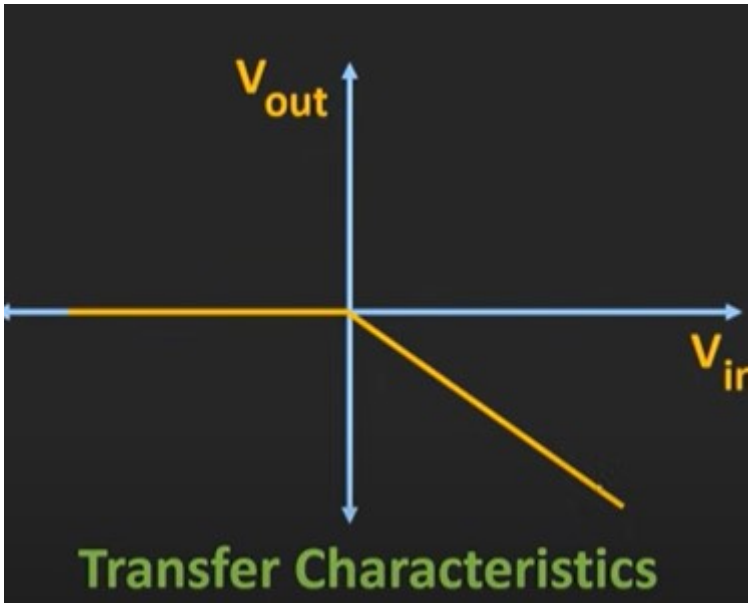






Output verses Input

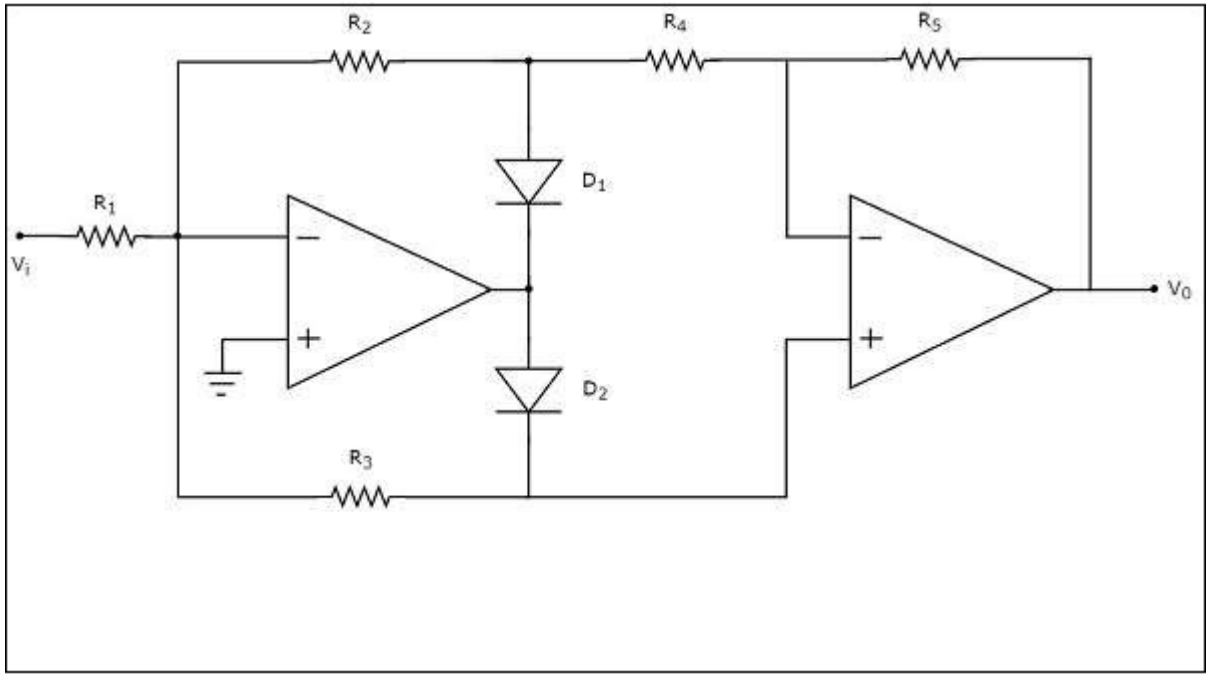




If $V_{in} > 0$, D1 is off, D2 is on, output V0= -(R2/R1)Vi

If $V_{in} < 0$, D1 is on, D2 is off, output V0= 0

Full wave Rectifier



The above circuit diagram consists of two op-amps, two diodes, D_1 & D_2 and five resistors, R_1 to R_5. For the **positive half cycle** of a sinusoidal input, the output of the first op-amp will be negative. Hence, diodes D_1 and D_2 will be forward biased and reverse biased respectively. Then, the output voltage of the first op-amp will be −

$$V_{01} = -\left(\frac{R_2}{R_1}\right) V_i$$

Observe that the output of the first op-amp is connected to a resistor R_4, which is connected to the inverting terminal of the second op-amp. The voltage present at the non-inverting terminal of second op-amp is 0 V. So, the second op-amp with resistors, R_4 and R_4 acts as an **inverting amplifier**.

The output voltage of the second op-amp will be

$$V_0 = -\left(\frac{R_5}{R_4}\right) V_{01}$$

Substituting the value of V_{01} in the above equation, we get –

$$=> V_0 = -\left(\frac{R_5}{R_4}\right)\left\{-\left(\frac{R_2}{R_1}\right) V_i\right\}$$

$$> V_0 = \left(\frac{R_2 R_5}{R_1 R_4}\right) V_i$$

Therefore, the output of a full wave rectifier will be a positive half cycle for the **positive half cycle** of a sinusoidal input. In this case, the gain of the output is $\frac{R_2 R_5}{R_1 R_4}$. If we consider $R_1 = R_2 = R_4 = R_5 = R$, then the gain of the output will be one.

For the **negative half cycle** of a sinusoidal input, the output of the first op-amp will be positive. Hence, diodes D_1 and D_2 will be reverse biased and forward biased respectively.

- The output voltage of the first op-amp will be −

$$V_{01} = -\left(\frac{R_3}{R_1}\right) V_i$$

The output of the first op-amp is directly connected to the non-inverting terminal of the second op-amp. Now, the second op-amp with resistors, R_4 and R_5 acts as a **non-inverting amplifier**.

The output voltage of the second op-amp will be −

$$V_0 = \left(1 + \frac{R_5}{R_4}\right) V_{01}$$

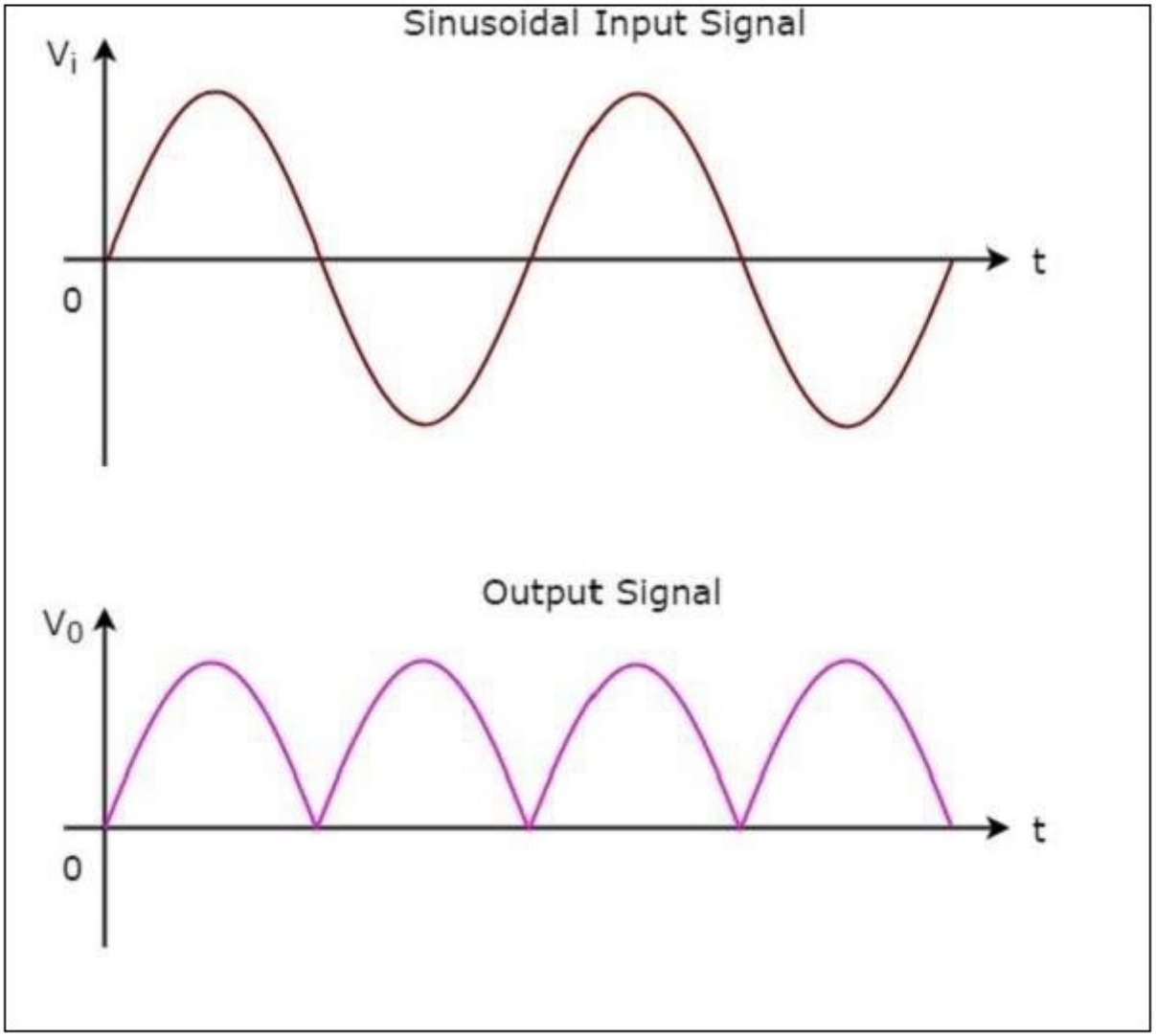
Substituting the value of V_{01} in the above equation, we get

$$=> V_0 = \left(1 + \frac{R_5}{R_4}\right) \left\{-\left(\frac{R_3}{R_1}\right) V_i\right\}$$

$$=> V_0 = -\left(\frac{R_3}{R_1}\right) \left(1 + \frac{R_5}{R_4}\right) V_i$$

- Therefore, the output of a full wave rectifier will be a **positive half cycle** for the negative half cycle of sinusoidal input also. In this case, the magnitude of the gain of the output is $\left(\frac{R_3}{R_1}\right) \left(1 + \frac{R_5}{R_4}\right)$. If we consider $R_1 = 2R_3 = R_4 = R_5 = R$ then the gain of the output will be **one**.

The **input** and **output waveforms** of a full wave rectifier are shown in the following figure



UNIT - III

Active Filters:

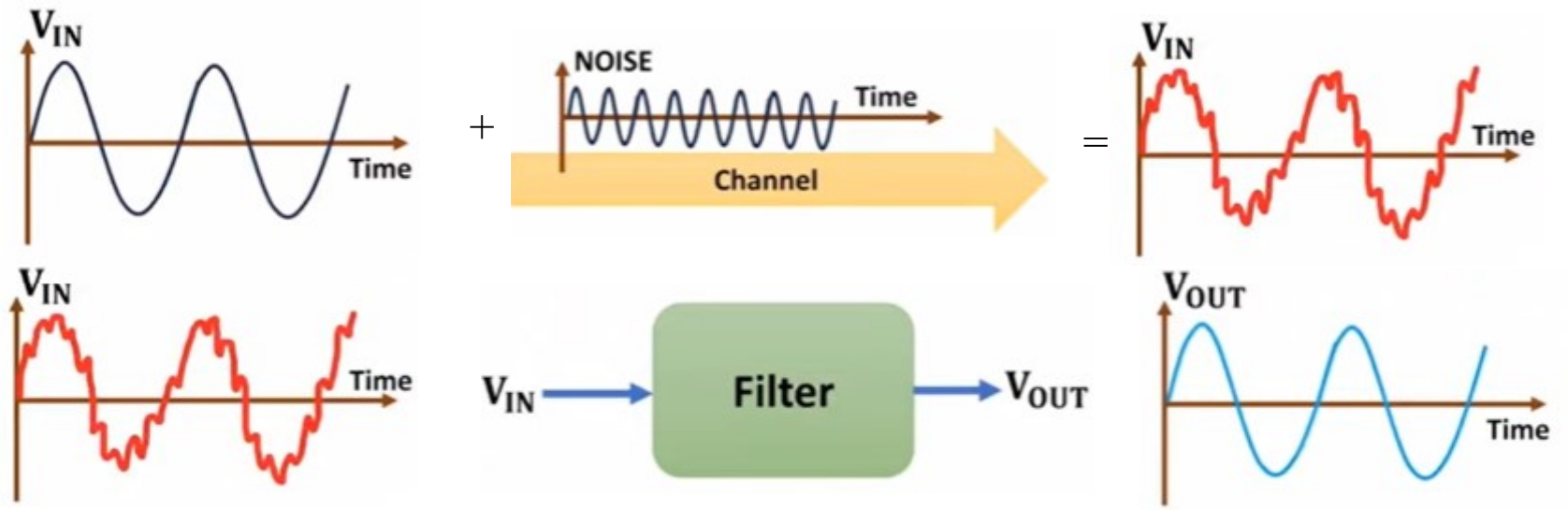
Filters are electronic circuits that allow certain frequency components and / or reject some other. It is used to separation of signals according to their frequencies. As their name implies, **Active Filters** contain active components such as operational amplifiers, transistors or FET's within their circuit design. Filters are widely used in communication and signal processing and network and sophisticated electronic instruments. They are passive and are the electric circuits or networks that consist of passive elements like resistor, capacitor, and (or) an inductor.
The main difference between a "passive filter" and an "active filter" is amplification.

Active filters design with passive component and active component like Op-amp, transistors etc.
Op amp have high input resistance and low output resistance. Because of these characteristics op amp used as a buffer to isolate the load from filter.

Active Filters

Basics of Filters in Electronics

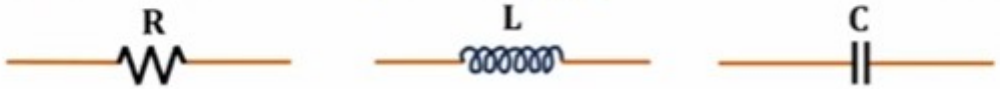
- It is a frequency-selective circuit.
- It allows a specific band of frequencies and blocks a specific band of frequencies.



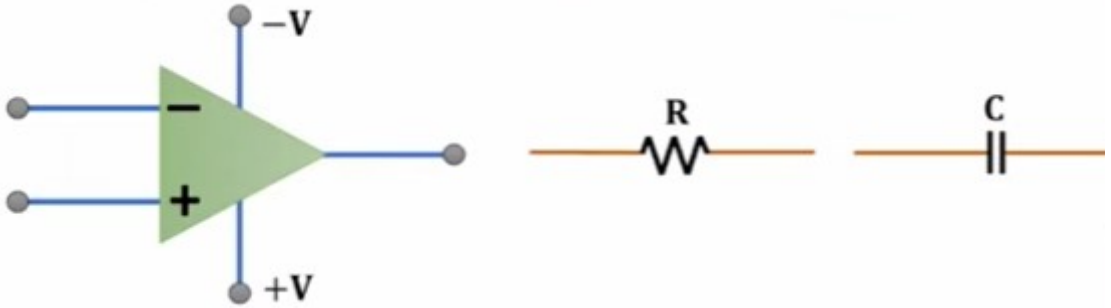
Input transmitting through channel(wired or wireless), it gets distorted. The distorted signal passing through filter, noise can removed and produce original signal without noise.

Active Filters Vs Passive Filters in Electronics

- Passive Filters don't need the power supply to work as filters. It is made up of R, C, and L.



- Typically, Inductors are not used in filters due to the following reasons.
  - Bulky in size
  - Dissipate more power
  - Emit Magnetic fields
  - Costly
- Active Filters need an additional power supply to work as filters.
- Active Filters can be effectively deployed using OpAmp, C and R.



Advantages of OpAmp in Filters

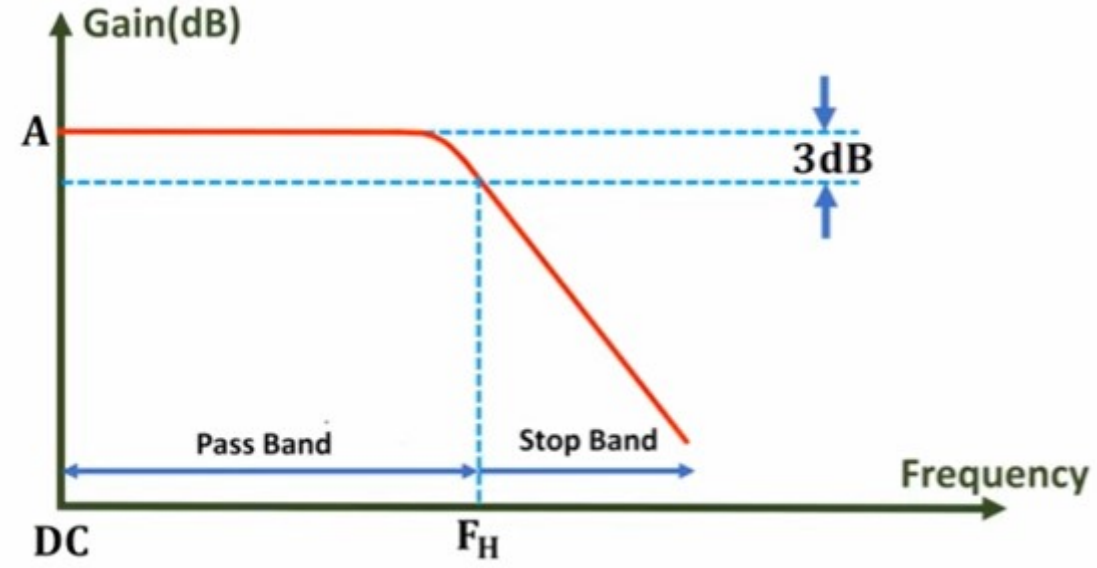
- OpAmp provides high gain, so the input signal does not attenuate during filtration.
- Active filters using OpAmp can be easily tuned to the required configuration.
- In passive filters, there can be a loading issue. Active filters using OpAmp have no loading problems.
- Cost-effective Active filters can easily be deployed using OpAmp.

Types of Filters

- Low Pass Filter
- High Pass Filter
- Band Pass Filter
  - Wide Band Pass Filter
  - Narrow Band Pass Filter
- Band Reject Filter/ Band Stop Filter
  - Wide Band Stop Filter
  - Narrow Band Stop Filter/ Notch Filter
- All Pass Filter

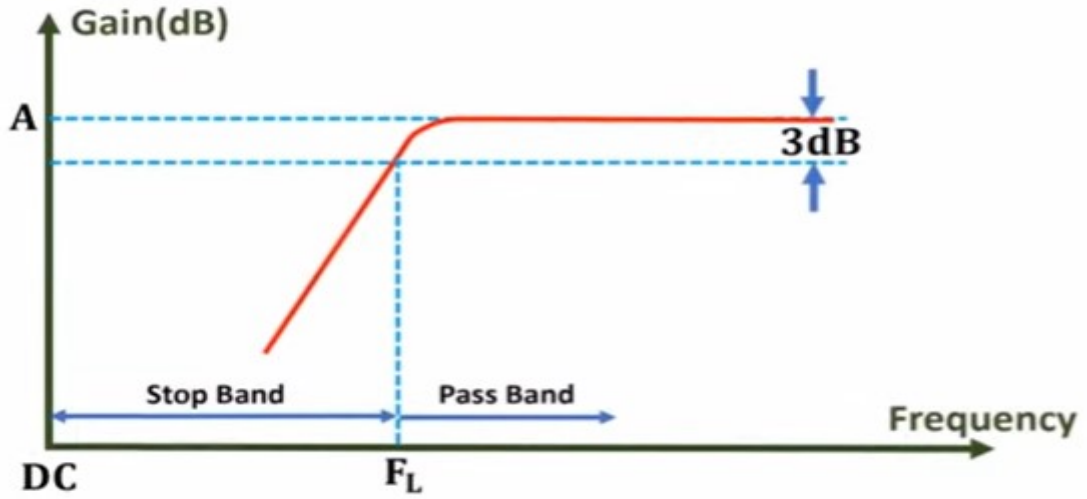
Low Pass Filter

- It passes low-frequency components through it and high-frequency components of the signal are blocked by LPF.



High Pass Filter

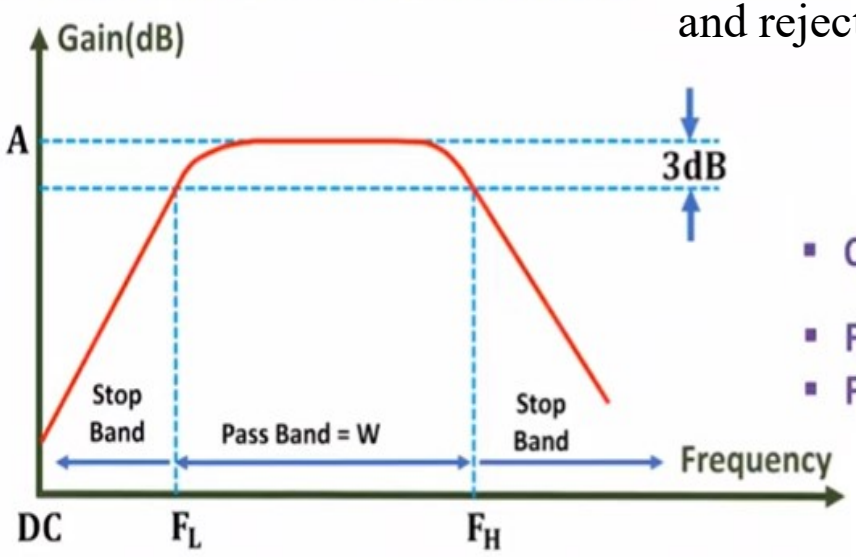
- It passes high-frequency components through it and low-frequency components of the signal are blocked by HPF.



Band Pass Filter

- It passes frequencies between F_L and F_H.

It allows to transmit certain(specific) band of frequencies and reject other frequencies components



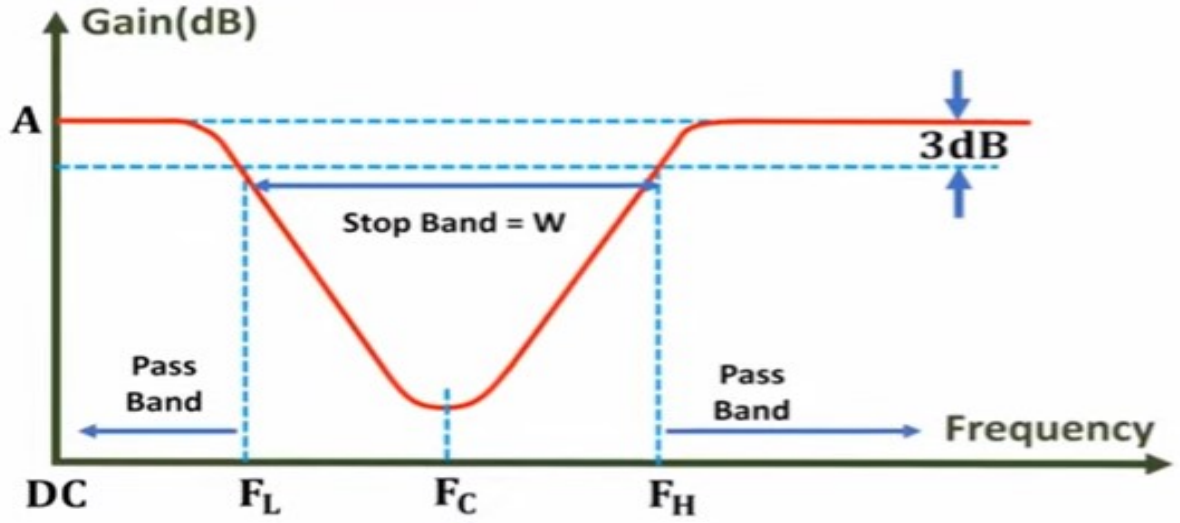
- Quality Factor $Q = \frac{F_C}{BW}$

FC is centre frequency
BW is bandwidth

- For wideband BSF, Q is lower {Usually, lower then 10}.
- For Narrowband BSF, Q is higher {Usually, higher then 10}.

Band Stop Filter/ Band Reject Filter

- It Blocks frequencies between F_L and F_H.



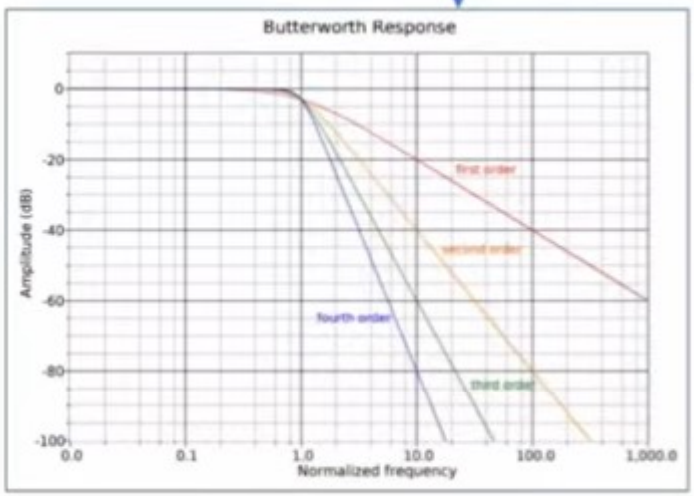
- Quality Factor $Q = \frac{F_C}{W}$
- For wideband BSF, Q is lower {Usually, lower then 10}.
- For Narrowband BSF, Q is higher {Usually, higher then 10}.

All Pass Filter

- It passes all the frequency components through it.
- It is used to correct the phase of signals.
- When signals are transmitted over transmission lines {Coaxial Cable, Twisted Pair, Optical Cable}, they undergo a change in phase.
- To compensate for the phase changes, we use the All Pass filter.
- Hence, The All Pass Filters are also known as Delay Equalizers or Phase Correctors.

Basics of 1st Order Butterworth Low Pass Filter

First Order Butterworth Low Pass Filter



It has a flat Passband Response.

It allows only Lower-frequency components to pass through it.

Types of Active Filters

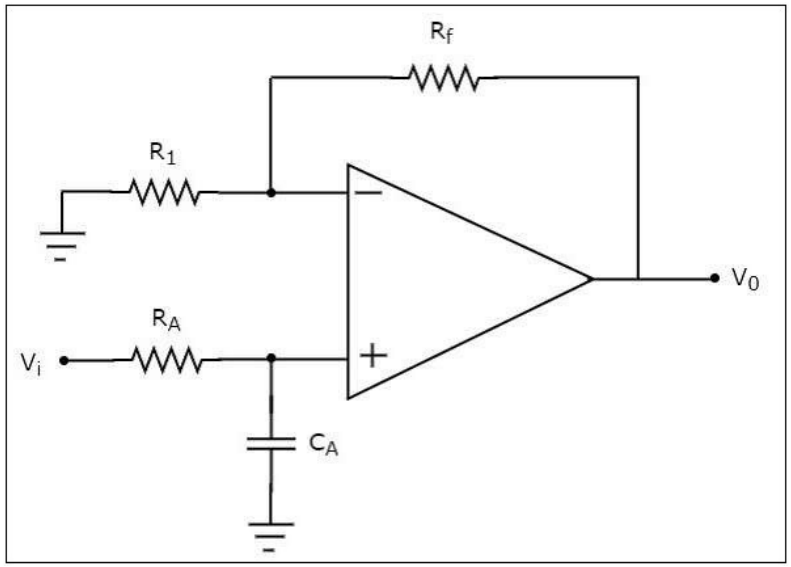
Active filters are the electronic circuits, which consist of active element like op-amp(s) along with passive elements like resistor(s) and capacitor(s). A frequency selective circuits that passes electric signals of specific band of frequencies and attenuate other frequencies.

Active filters are mainly classified into the following **four types** based on the band of frequencies that they are allowing and / or rejecting −

- Active Low Pass Filter
- Active High Pass Filter
- Active Band Pass Filter
- Active Band Stop Filter

Active Low Pass Filter:

If an active filter allows (passes) only **low frequency** components and rejects (blocks) all other high frequency components, then it is called as an **active low pass filter**.



The most common and easily understood active filter is the **Active Low Pass Filter**. Its principle of operation and frequency response is exactly the same as those for the previously seen passive filter, the only difference this time is that it uses an op-amp for **amplification and gain control**.

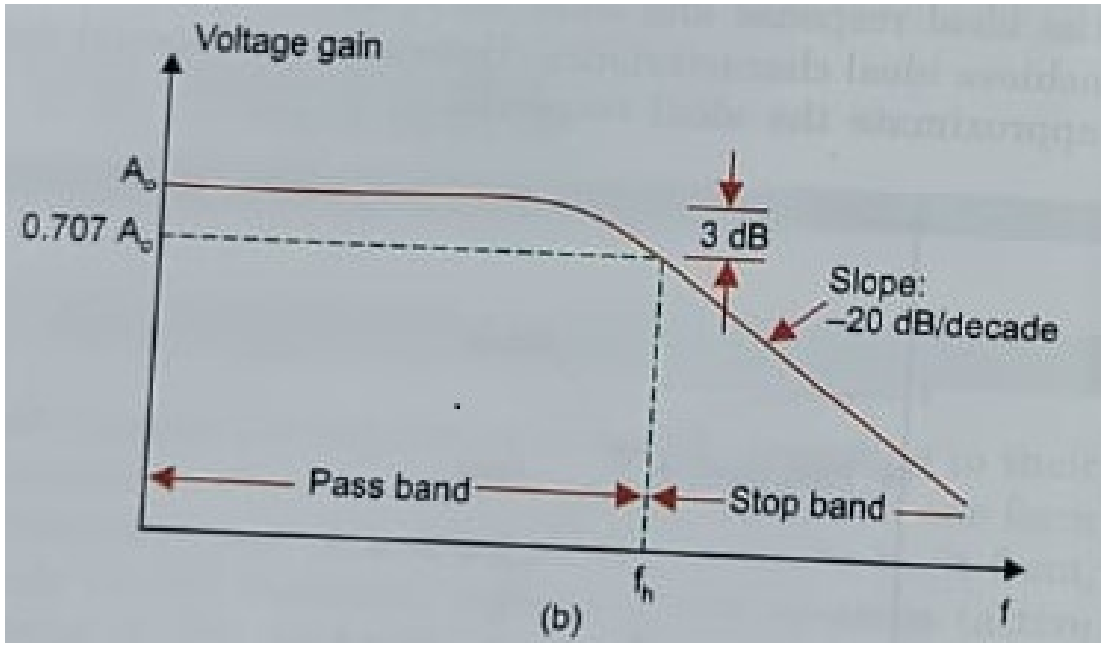
This first-order low pass active filter, consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. So, the input of a non-inverting terminal of an op amp is the output of a passive low pass filter.

Observe that the above circuit resembles a **non-inverting amplifier**. It is having the output of a passive low pass filter as an input to the non-inverting terminal of op-amp.

Hence, it produces an output,

which is $\left(1+\frac{R_f}{R_1}\right)$ times the input present at the non-inverting terminal.

We can choose the values of R_f and R_1 suitably in order to obtain the **desired gain** at the output. Suppose, if we consider the resistance values of R_f and R_1 as zero ohms and infinity ohms, then the above circuit will produce a **unity gain** low pass filter output.



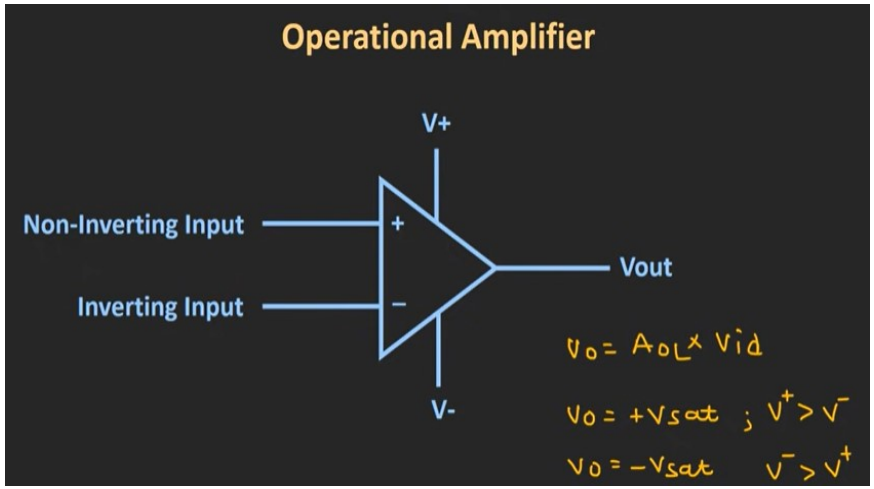
WAVEFORM GENERATORS

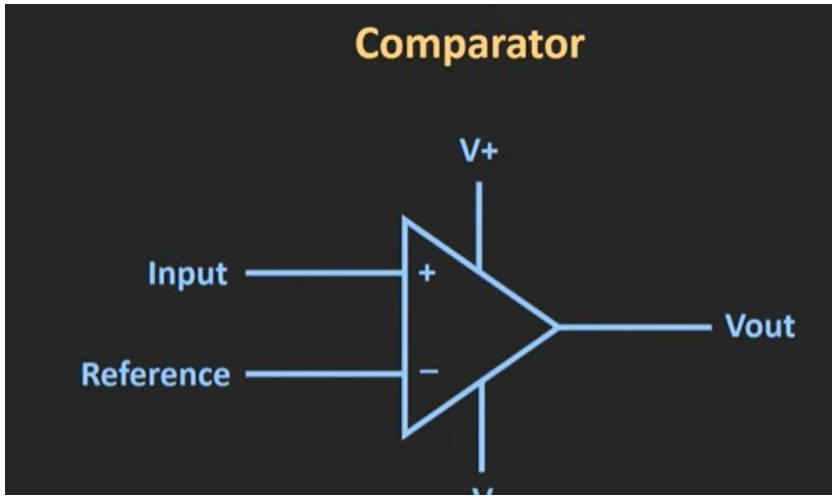
WAVEFORM GENERATORS: The various op-amp circuits used for generating various waveforms such as square, triangular, saw tooth, sine etc. are called signal generators or waveform generators. Waveform generators produce a time dependent signals with required frequency, amplitude and wave shape.

Comparator : A **comparator** is an electronic circuit, which compares the two inputs that are applied to it input terminals and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser. Basically it is open loop op amp and operates in a non-linear manner.

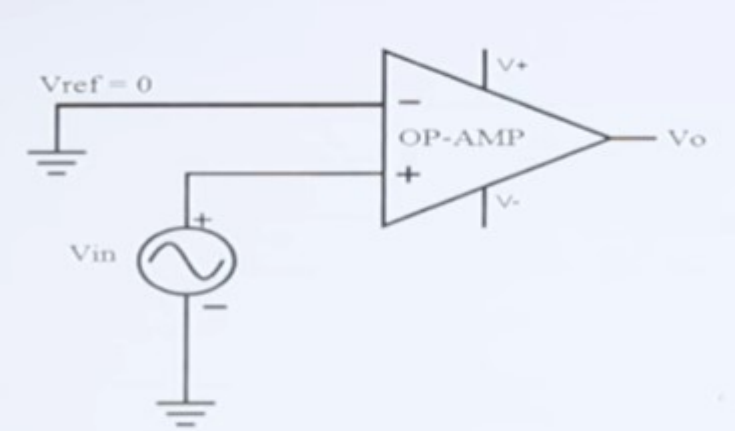
Applications:

Zero crossing detector, Window detector, Time marker generator, Phase meter

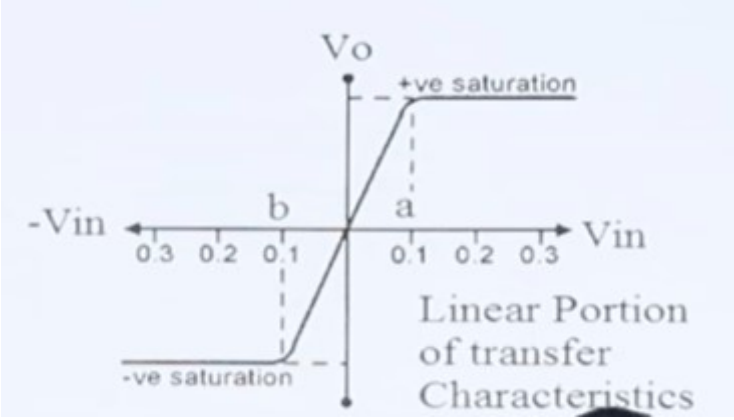




Op-Amp as a Comparator

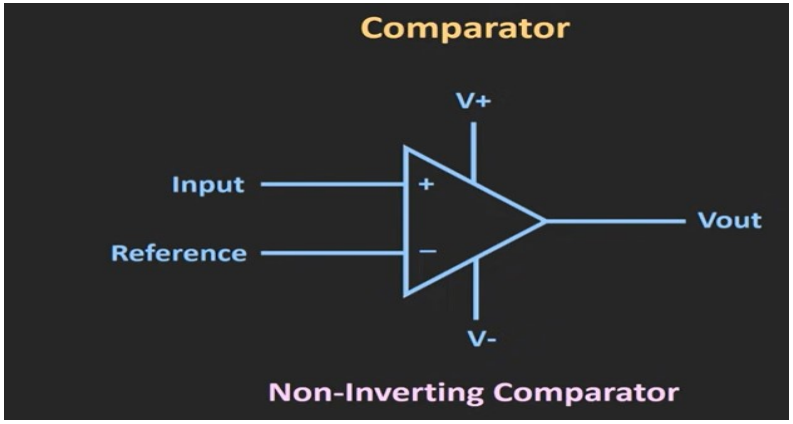


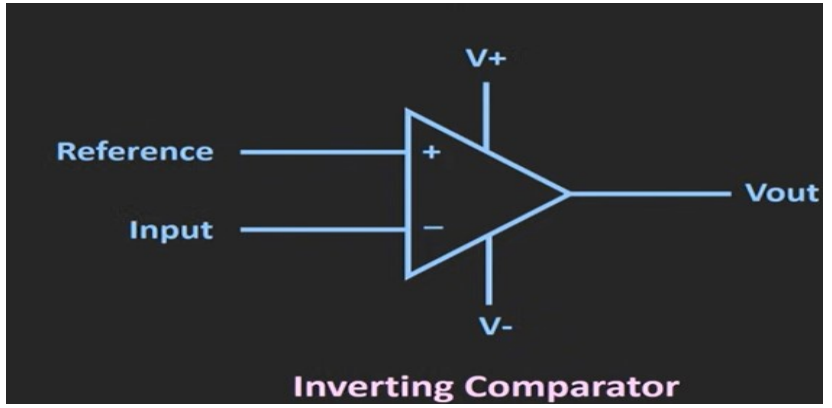
Basic Comparator Circuit



Transfer Characteristics

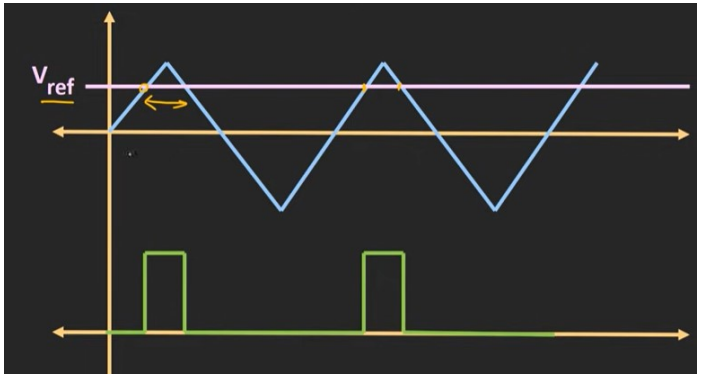
Comparators are of two types : **Inverting** and **Non-inverting comparators**.

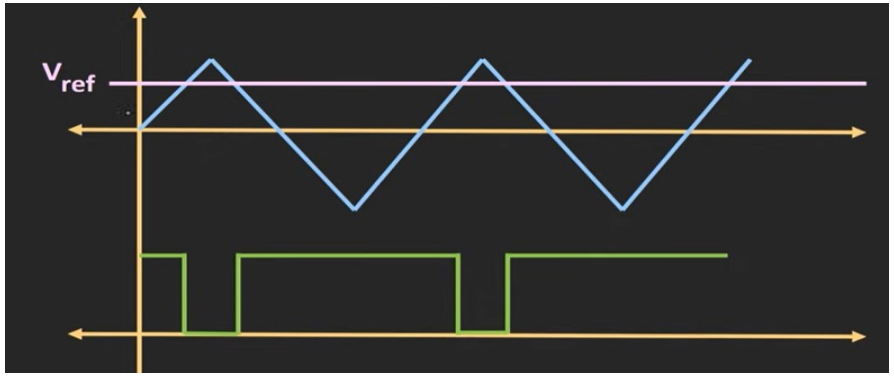


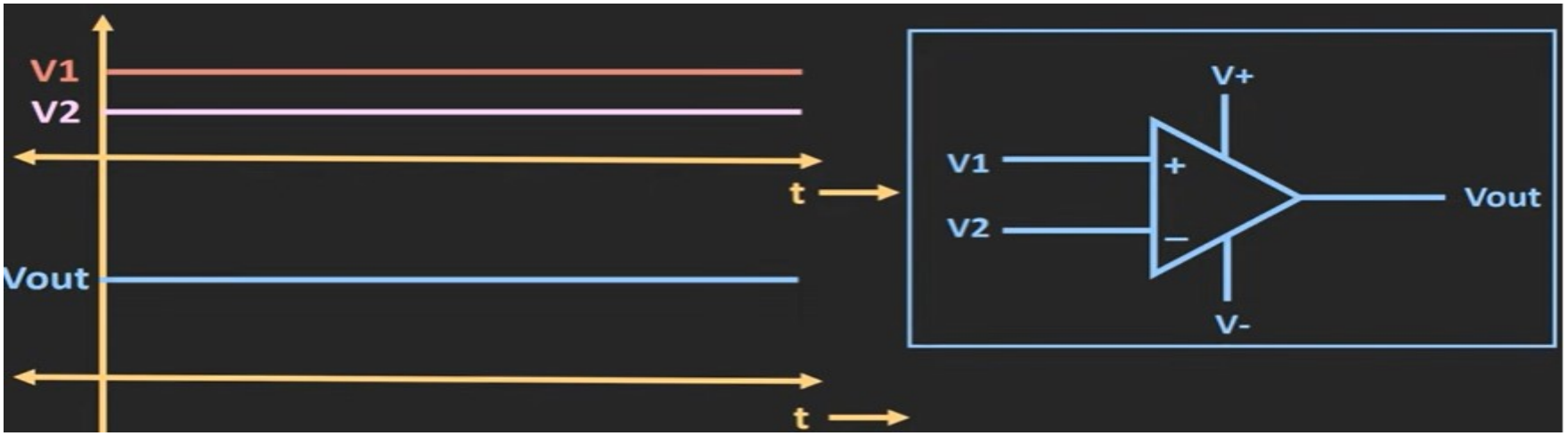


If the input is applied at the non inverting terminal of op amp, this comparator is called non inverting comparator. Input is goes above the reference value, the output of comparator should be high.

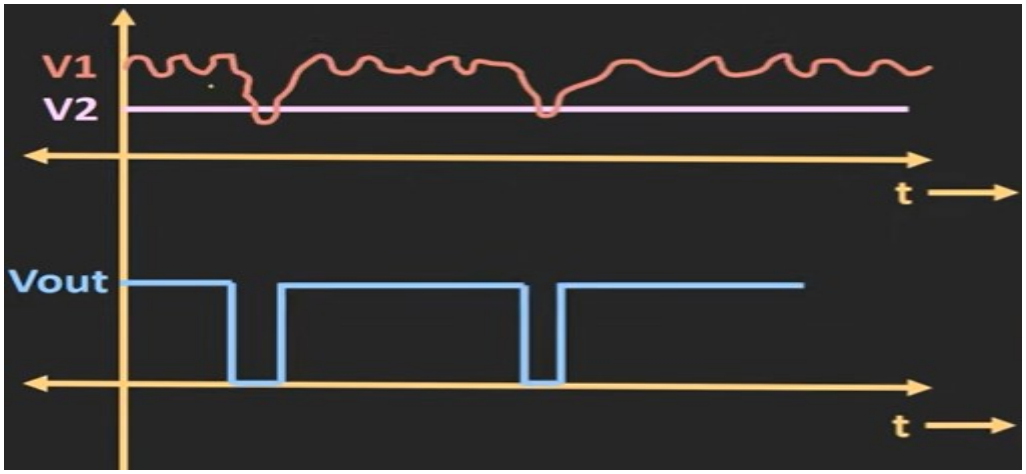
If the input is applied at inverting terminal of op amp, this comparator is called inverting comparator. Input is goes beyond the reference value, the output of comparator should be low.







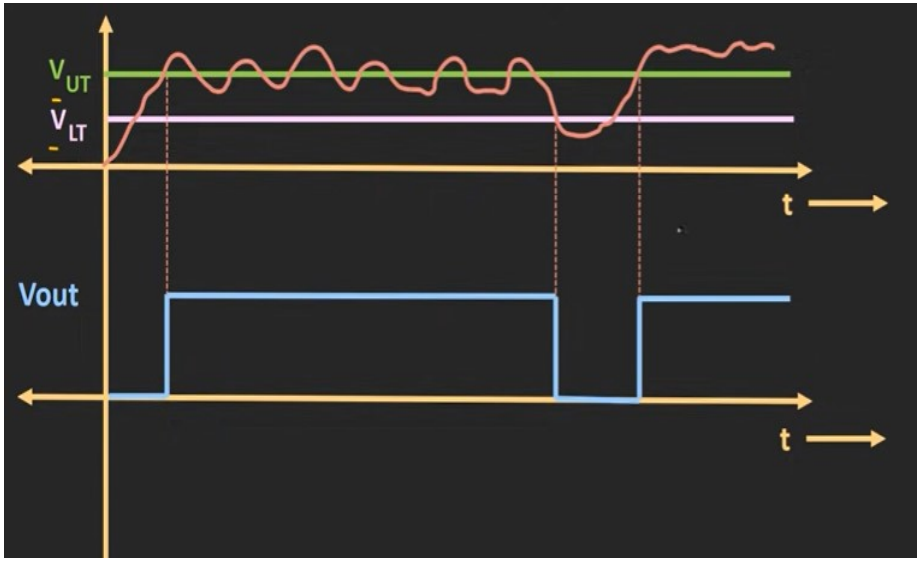
If the input (V1) is greater than V2, output is high, if V1 effected by noisy, the out should be affected , it shown in below figure. We can say comparator is not immune to noise. This problem can be avoided by Schmitt trigger. It is noting but comparator with hysteresis.

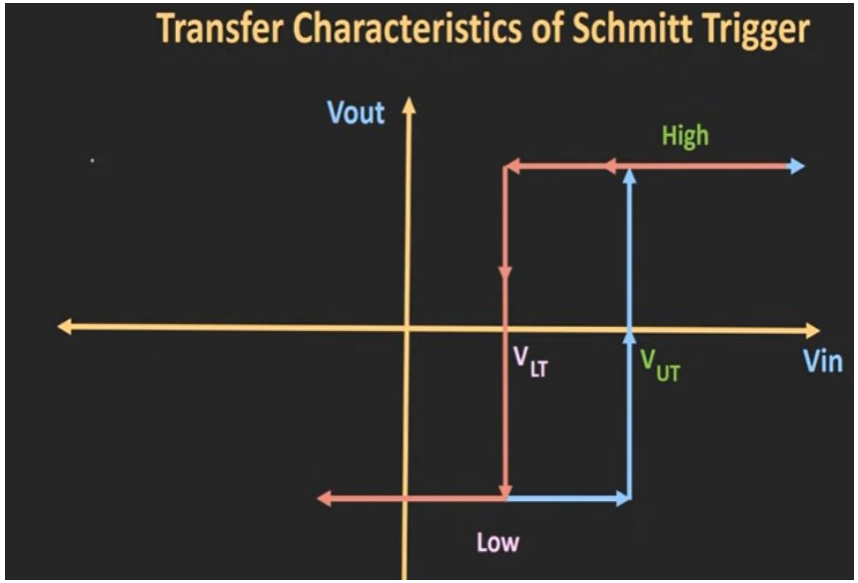


Schmitt trigger (Regenerative Comparator): Comparator with positive feedback is called Schmitt trigger. Because of +ve feedback it is called Regenerative circuit.

It is nothing but comparator with hysteresis. It has two threshold voltages. One upper threshold voltage for low to high transition and other is lower threshold voltage for high to low transition. It provide noise immunity between UTP and LTP.

The difference between upper and lower threshold voltage is known as hysteresis voltage of schmitt trigger. Hysteresis voltage defines the noise immunity of the schmtt trigger.





If the input is less than UTP, the output will be low and input crosses UTP, the output become high. If the input start to reduce, the output should high up to the input is below the LTP. If input cross LTP and below the LTP, output become low.

Inverting Schmitt trigger :

Schmitt Trigger :

- Also Called 'Regenerative Comparator'
- If positive feedback added to Comparator circuit, gain can be increased greatly.
- Theoretically, loop gain $-\beta A_{OL}$ adjusted to Unity, then 'A_{vf}' becomes '∞'. So, abrupt transitions at o/p.
- Practically, Unity gain is not possible due to variations in Supply voltage & Temp.
- So, gain > Unity is chosen.

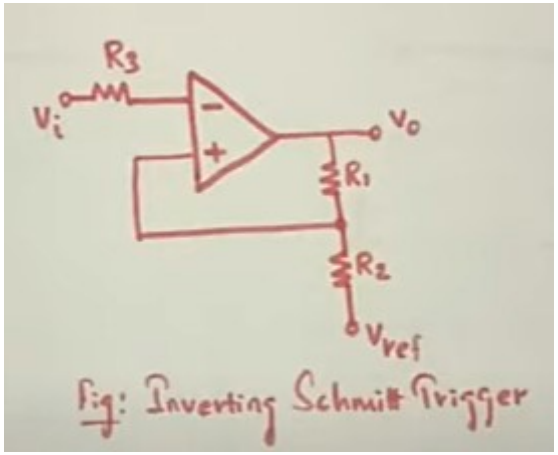
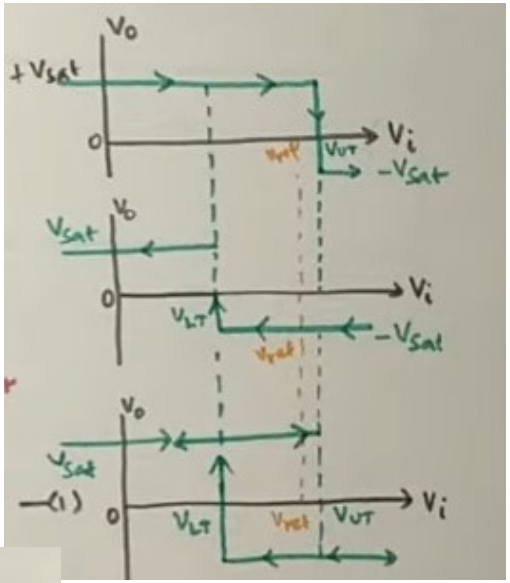


Fig: Inverting Schmitt Trigger

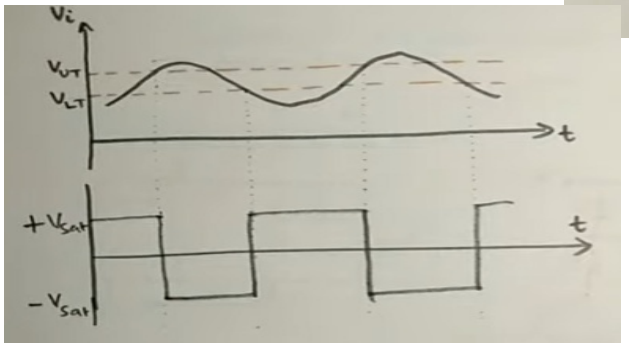
$R_3 = R_1 \| R_2$
To Compensate I/P Bias current



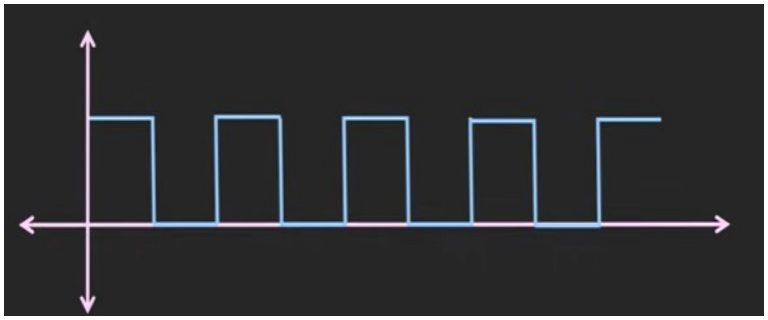
$$V_{UT} = \frac{V_{ref} \cdot R_1}{R_1 + R_2} + \frac{V_{sat} \cdot R_2}{R_1 + R_2} \quad \text{—(1)}$$

$$V_{LT} = \frac{V_{ref} \cdot R_1}{R_1 + R_2} - \frac{V_{sat} \cdot R_2}{R_1 + R_2} \quad \text{—(2)}$$

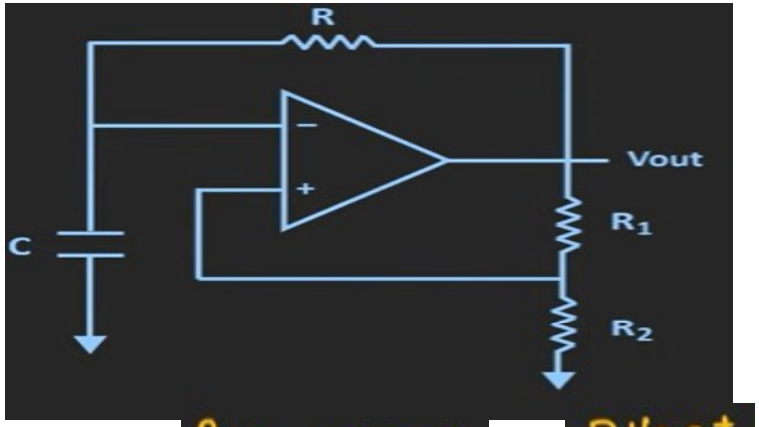
$$V_H = V_{UT} - V_{LT} = \frac{2 V_{sat} \cdot R_2}{R_1 + R_2} \quad \text{—(3)}$$



Astable Multivibrator

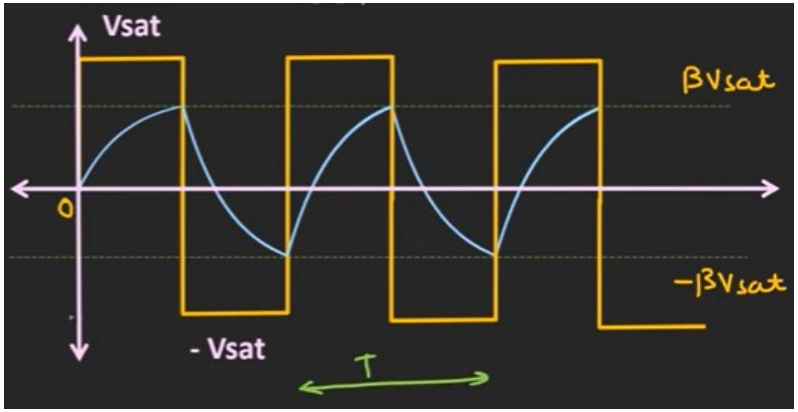


In astable multivibrator, both the states are astable (no stable), output continuously change between two states. It is also called free running oscillator or relaxiation oscillator (it means output is non sinusoidal). The astable multivibrator is an oscillator which produces a square wave output voltage. Its frequency can be controlled by changing the R and C values. It is realize by op amp with positive feedback as shown in fig. =



$$\frac{R_2}{R_1+R_2} \times V_{sat} = \beta V_{sat}$$

$$T = 2RC \times \ln\left(\frac{1+\beta}{1-\beta}\right)$$



Advantages of Astable Multivibrator

No external triggering required.
Circuit design is simple.
Inexpensive.
Can function continuously.

Disadvantages of Astable Multivibrator

Energy absorption is more within the circuit.
Output signal is of low energy.
Duty cycle less than or equal to 50% can't be achieved.

Astable multivibrators

These are used in:

- Timing circuits: Used in digital clocks, timers, and delay circuits
- Pulse generation: Used to generate clock pulses for synchronous generators
- Oscillators: Used to generate waveforms for audio and RF applications
- Amateur radio equipment: Used in amateur radio equipment
- Morse code generators: Used in Morse code generators
- Analog circuits: Used in analog circuits
- TV systems: Used in TV systems

Advantages of Monostable Multivibrator

Provides fixed-duration pulses independent of the trigger pulse width.
Simple circuit design using only 2 transistors, 1 capacitor and few resistors.
Timing parameters can be adjusted by varying resistor and capacitor values.
Timing is highly accurate due to the use of RC network for timing.
Very useful for applications requiring pulse generation or one-shot pulse triggering.

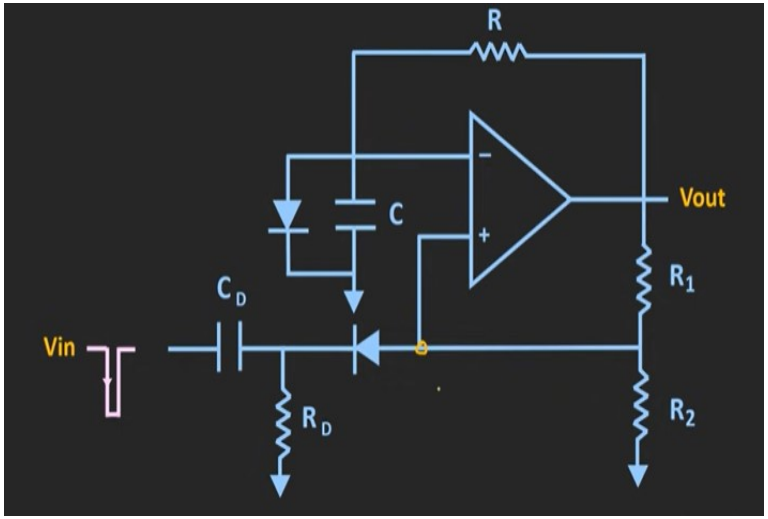
Disadvantages of Monostable Multivibrator

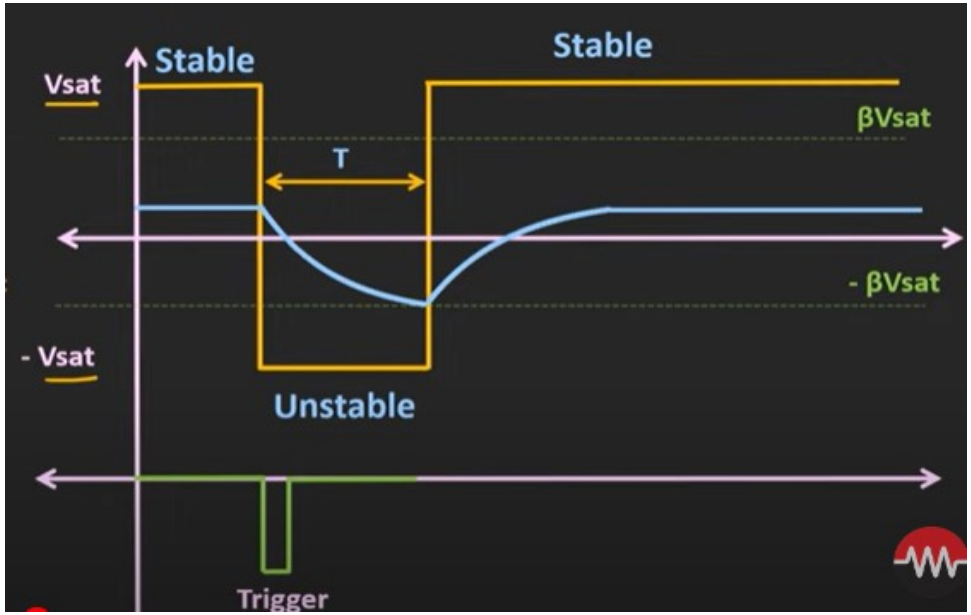
Despite its advantages, the monostable multivibrator has some limitations:
External Trigger Requirement: Needs an external trigger to operate.
Pulse Width Dependency: The output pulse width is fixed based on the RC components, limiting flexibility.

Monostable multivibrators
These are used in:

- •Timing circuits: Used in timers, delay circuits, and clock pulse generation
- •Pulse shaping: Used to convert irregular pulses into uniform ones
- •Switch debouncing: Used to remove noise from mechanical switches
- •Frequency division: Used in digital frequency dividers
- •Regeneration of distorted waves: Used to regenerate distorted waves
- •Control of output signal frequency: Used to control an output signal frequency in analog systems

Monostable Multivibrator





$$V_{C(t)} = V_{Final} + (V_{initial} - V_{Final})\, e^{-t/RC}$$

$V_{Final} = -V_{sat}$

$V_{initial} = 0V$

$$V_C(t_1) = -V_{sat} + (0 - (-V_{sat}))\, e^{-t_1/RC}$$

$$-\beta V_{sat} = -V_{sat} + V_{sat}\, e^{-t_1/RC}$$

$$\therefore \quad 1 - \beta = e^{-t_1/RC}.$$

$$1 - \frac{R_2}{R_1+R_2} = e^{-t_1/RC}$$

$$\therefore \quad \frac{R_1}{R_1+R_2} = e^{-t_1/RC}$$

$$\therefore \quad t_1 = -RC \ln\left(\frac{R_1}{R_1+R_2}\right)$$

$$\therefore \quad t_1 = RC \ln\left(1 + \frac{R_2}{R_1}\right)$$

Triangular wave Generator

A triangular wave generator is an electronic circuit, which generates a triangular wave. The **block diagram** of a triangular wave generator is shown in figure.

The block diagram of a triangular wave generator contains mainly two blocks: a square wave generator and an integrator. These two blocks are **cascaded**. That means, the output of square wave generator is applied as an input of integrator. Note that the integration of a square wave is nothing but a triangular wave. The triangular wave is generated by alternatively charging and discharging a capacitor with a constant current. This is achieved by connecting integrator circuit at the output of square wave generator. Assume that V' is high at $+V_{sat}$.

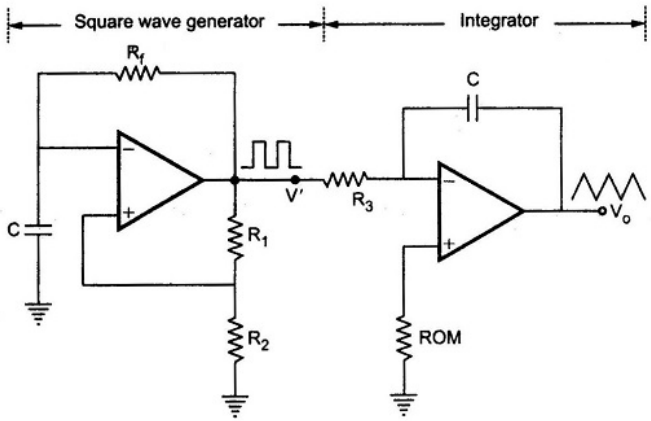


Fig. 2.85 Triangular wave generator

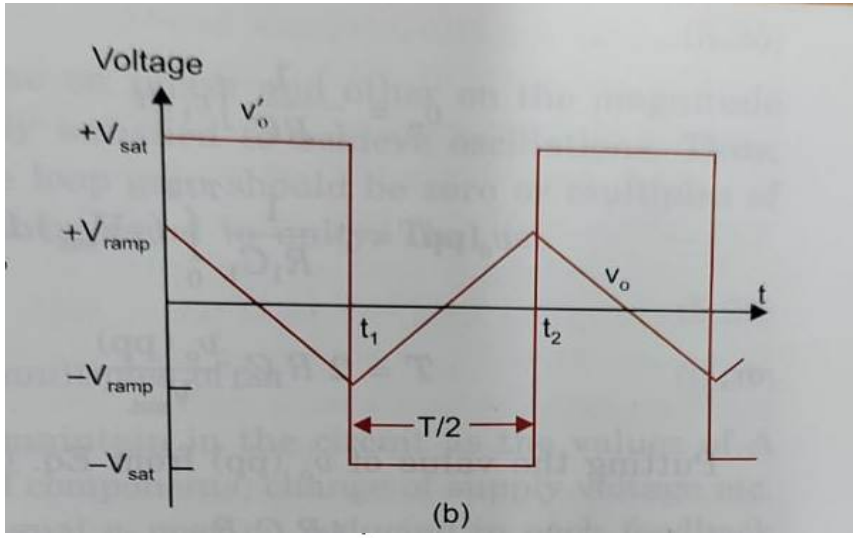


Fig. 2.86 Waveforms of triangular wave generator

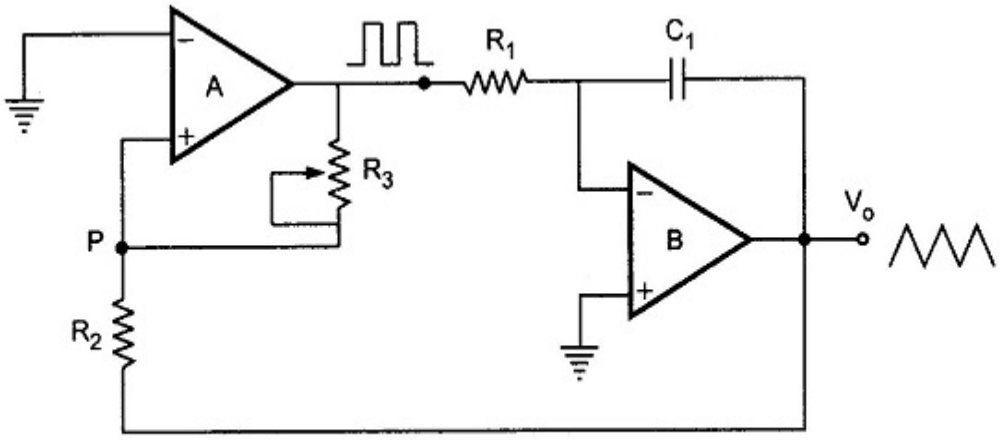
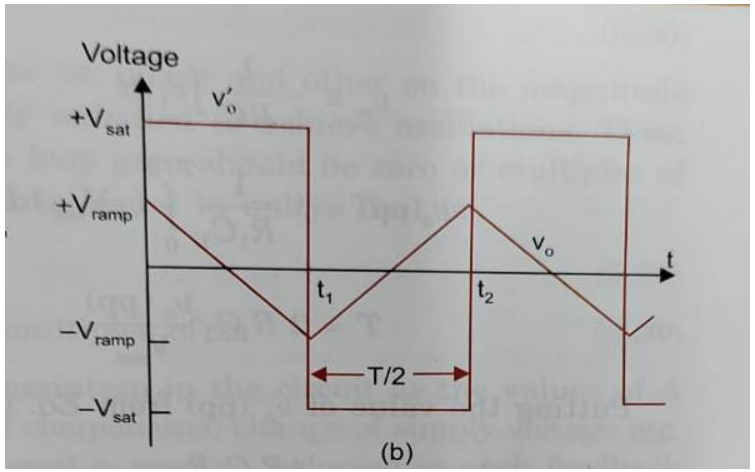


Fig. 2.88 Triangular wave generator



It consists of a comparator (A) and an integrator (B). The output of comparator A is a square wave of amplitude ± V_{sat} and is applied to the inverting (-) input terminal of the integrator B. The output of integrator is a triangular wave and it is feedback as input to the comparator A through a voltage divider R_2 R_3.

To understand circuit operation, assume that the output of comparator A is at + V_{sat} . This forces a constant current (+ V_{sat}/R_1) through C to give a negative going ramp at the output of the integrator, as shown in the Fig. 2.88. Therefore, one end of voltage divider is at a voltage +V_{sat} and the other at the negative going ramp. When the negative going ramp reaches a certain value -V_{ramp}, the effective voltage at point p becomes slightly below 0V. The output of the comparator is transition from +Vsat to –Vsat. This forces a constant current (- V_{sat}/R_1) through C to give a positive going ramp at the output of the integrator.

Amplitude and Frequency Calculations:

The frequency and amplitude of the Triangular Wave Generator Using Op amp wave can be determined as follows :

When comparator output is at $+V_{sat}$, the effective voltage at point P is given by

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] \quad \ldots (1)$$

When effective voltage at P becomes equal to zero, we can write above equation as,

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] = 0$$

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}(V_{ramp}) + \frac{R_2}{R_2 + R_3}(+V_{sat}) = 0$$

$$\frac{-R_3}{R_2 + R_3}(V_{ramp}) = -\frac{R_2}{R_2 + R_3}(+V_{sat})$$

$$\therefore \quad -V_{ramp} = \frac{-R_2}{R_3}(+V_{sat}) \quad \ldots (2)$$

Similarly, when comparator output is at $-V_{sat}$, we can write,

$$V_{ramp} = \frac{R_2}{R_3}(-V_{sat}) \quad \ldots (3)$$

The peak to peak amplitude of the triangular wave can be given as

$$V_{o(pp)} = +V_{ramp} - (-V_{ramp}) \quad \text{... (4)}$$

$$= \frac{-R_2}{R_3}(-V_{sat}) - \left(\frac{-R_2}{R_3}\right)(+V_{sat})$$

If $|+V_{sat}| = |-V_{sat}|$ then, we can write

$$V_{o(pp)} = \frac{R_2}{R_3} V_{sat} + \frac{R_2}{R_3} V_{sat} = \frac{2R_2}{R_3} V_{sat} \quad \text{... (5)}$$

The time taken by the output to swing from $-V_{ramp}$ to $+V_{ramp}$ (or from $+V_{ramp}$ to $-V$ is equal to half the time period T/2. Refer Fig. 2.89. This time can be calculated fro integrator output equation as follows :

$$V_{o(pp)} = -\frac{1}{R_1 C_1}\int_0^{T/2} (-V_{sat})\, dt = \left(\frac{V_{sat}}{R_1 C_1}\right)\frac{T}{2} \quad \text{... (6)}$$

$$T = \frac{2R_1 C_1 V_{o(pp)}}{V_{sat}} \quad \text{.... (7)}$$

Substituting value of $V_{o(pp)}$ we get,

$$T = \frac{2R_1 C_1\left(\frac{2R_2}{R_3} V_{sat}\right)}{V_{sat}} = \frac{4R_1 C_1 R_2}{R_3} \quad \text{... (8)}$$

Therefore, the frequency of oscillation can be given as,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1 C_1 R_2} \quad \text{... (9)}$$

Oscillator

An oscillator is a circuit that produces periodic electric signals such as sine wave or square wave. The application of oscillator includes sine wave generator, local oscillator for synchronous receivers etc. An oscillator consists of an amplifier and a feedback network.

1. 'Active device' i.e. opamp is used as an amplifier.
2. Passive components such as R-C or L-C combinations are used as feedback network.

To start the oscillation with the constant amplitude, positive feedback is not the only sufficient condition. Oscillator circuit must satisfy the following two conditions known as **Barkhausen** conditions:

1. Magnitude of the loop gain $(A_v \beta) = 1$,

   where, A_v = Amplifier gain and
   β = Feedback gain.

2. Phase shift around the loop must be 360° or 0°.

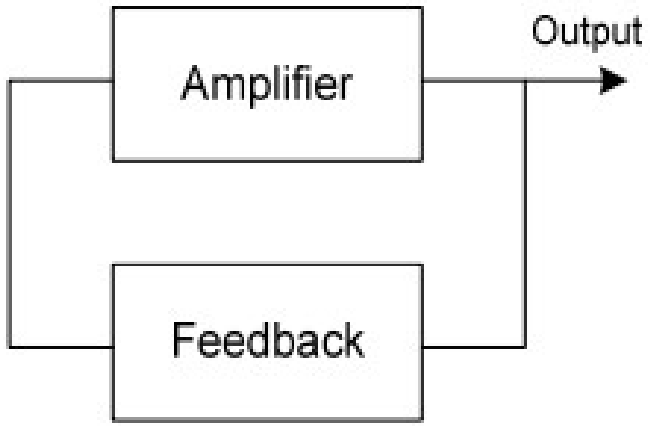


Fig 1. Basic oscillator block diagram

RC Phase Shift Oscillator Using Op amp

RC Phase Shift Oscillator basically consists of an amplifier and a feedback network consisting of resistors and capacitors. R-C phase shift oscillator using op-amp uses op-amp in inverting amplifier mode. Thus it introduces the phase shift of 180° between input and output. The feedback network consists of 3 RC sections each producing 60° phase shift. Such a RC phase shift oscillator using op-amp is shown in the Fig.

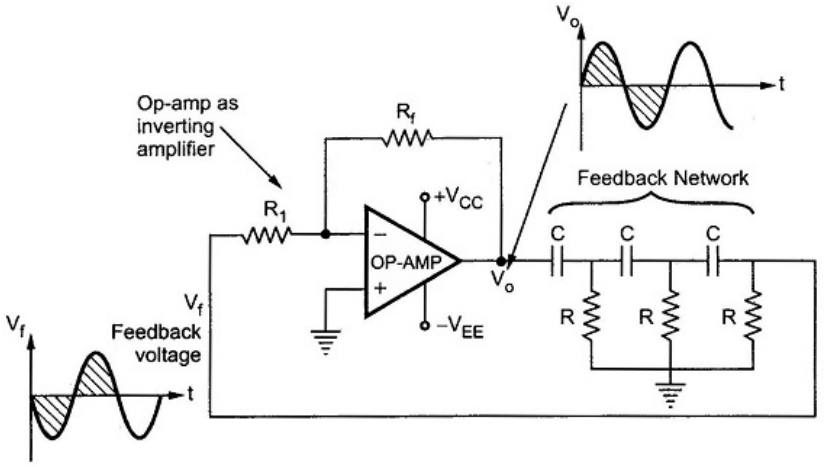


Fig. 2.92 R-C Phase shift oscillator using op-amp

The output of amplifier is given to feedback network. The Output of feedback network drives the amplifier. The total phase shift around a loop is 180° of amplifier and 180° due to 3 RC section, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

The frequency of sustained oscillations generated depends on the values of R and C and is given by,

$$f = \frac{1}{2\pi\sqrt{6}\,RC}$$

The frequency is measured in Hz.

At this frequency the gain of the op-amp must be at least 29 to satisfy Aβ = 1.

Now gain of the op-amp inverting amplifier is given by,

$$|A| \geq \frac{R_f}{R_1} \geq 29 \text{ for oscillations}$$

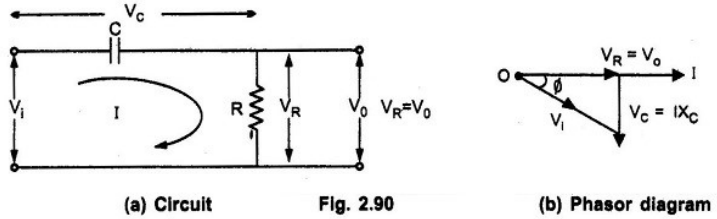
$$\therefore \quad R_f \geq 29\, R_1$$

Thus circuit will work as an oscillator which will produce a sinusoidal waveform if gain is 29 and total phase shift around a loop is 360°. This satisfies the Barkhausen criterion for the oscillator. These oscillators are used over the audio frequency range i.e. about 20 Hz upto 100 kHz.

$$I = \frac{V_i \angle 0°}{Z} = \frac{V_i \angle 0°}{|Z| \angle -\phi}$$

$$\therefore \quad I = \frac{V_i}{Z} \angle +\phi \quad A$$

$$\phi = \tan^{-1}\left(\frac{X_C}{R}\right)$$



(a) Circuit Fig. 2.90 (b) Phasor diagram

From expression of current it can be seen that current I leads input voltage V_i by angle Φ.

RC network is used in feedback path. In oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°. RC network is used in feedback path. In oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°.

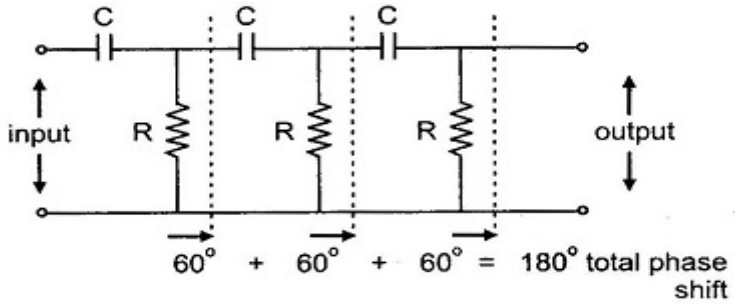


Fig. 2.91 Feedback network in RC phase shift oscillator

Advantages of RC Phase Shift Oscillator:

The Advantages of RC Phase Shift Oscillator are,

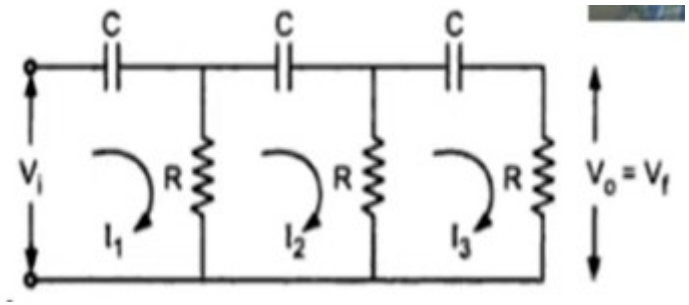
1. The circuit is simple to design.
2. Can produce output over audio frequency range.
3. Produces sinusoidal output waveform.
4. It is a fixed frequency oscillator.

Disadvantages of RC Phase Shift Oscillator:

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

Derivation for frequency of oscillations:

- Consider the feedback network
- Apply KVL to the loops



$$I_1\left(R+\frac{1}{j\omega C}\right)-I_2 R = V_i \quad \text{--- (1)}$$

$$-I_1 R+I_2\left(2R+\frac{1}{j\omega C}\right)-I_3 R = 0 \quad \text{--- (2)}$$

$$0-I_2 R+I_3\left(2R+\frac{1}{j\omega C}\right) = 0 \quad \text{--- (3)}$$

- Replace jw as S and using matrix form,

$$\begin{bmatrix} R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{bmatrix}\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_i \\ 0 \\ 0 \end{bmatrix} \quad \text{--- (4)}$$

- Solving the above matrix for I_3 using Cramer's rule.

$$I_3 = \frac{D_3}{D} = \frac{V_i R^2 s^3 C^3}{1 + 5\,sRC + 6\,s^2C^2R^2 + s^3C^3R^3} \quad \text{--- (5)}$$

$$V_o = V_f = I_3 R = \frac{V_i R^3 s^3 C^3}{1 + 5\,sRC + 6\,s^2C^2R^2 + s^3C^3R^3} \quad \text{--- (6)}$$

$$\beta = \frac{V_o}{V_i}$$

$$= \frac{R^3 s^3 C^3}{1 + 5\,sCR + 6\,s^2C^2R^2 + s^3C^3R^3}$$

Replacing s by $j\omega$, s^2 by $-\omega^2$, s^3 by $-j\omega^3$

$$\beta = \frac{-j\omega^3 R^3C^3}{1 + 5\,j\omega CR - 6\,\omega^2C^2R^2 - j\omega^3C^3R^3}$$

Dividing numerator and denominator by $-j\omega^3 R^3C^3$ and using,

$$\alpha = \frac{1}{\omega RC}$$

$$\beta = \frac{1}{(1 - 5\alpha^2) + j\alpha(6 - \alpha^2)}$$

- Equating imaginary part to zero to find the frequency of oscillations.

$$\alpha(6-\alpha^2) = 0$$

$$\alpha^2 = 6$$

$$\alpha = \sqrt{6}$$

$$\frac{1}{\omega RC} = \sqrt{6}$$

$$\omega = \frac{1}{RC\sqrt{6}}$$

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

Where, f is frequency of oscillations.

- At this frequency

$$\beta = \frac{1}{1-5\times(\sqrt{6})^2} = -\frac{1}{29} \qquad |\beta| = \frac{1}{29}$$

$$|A|\ |\beta| \geq 1$$

$$|A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{29}\right)}$$

$$\boxed{|A| \geq 29}$$

- For oscillations to occur, the gain of the op-amp must be ≥29. which can be adjusted by the resistors R_f & R_1

Wien Bridge Oscillator :

Another type of popular audio frequency oscillator is the Wien bridge oscillator circuit. This is mostly used because of its important features. This circuit is free from the **circuit fluctuations** and the **ambient temperature**. The main advantage of this oscillator is that the frequency can be varied in the range of 10Hz to about 1MHz whereas in RC oscillators, the frequency is not varied.

Wien bridge oscillator is an audio frequency sine wave oscillator of high stability and simplicity. It consists of balanced bridge used as feedback network. The circuit can be viewed as a Wien bridge with lead-lag network i.e. series combination of R1 and C1 in one arm and parallel combination of R2 and C2 in the adjoining arm and voltage divider i.e. Resistors R3 and R4 are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge. The feedback signal in this circuit is connected to the non-inverting input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift.

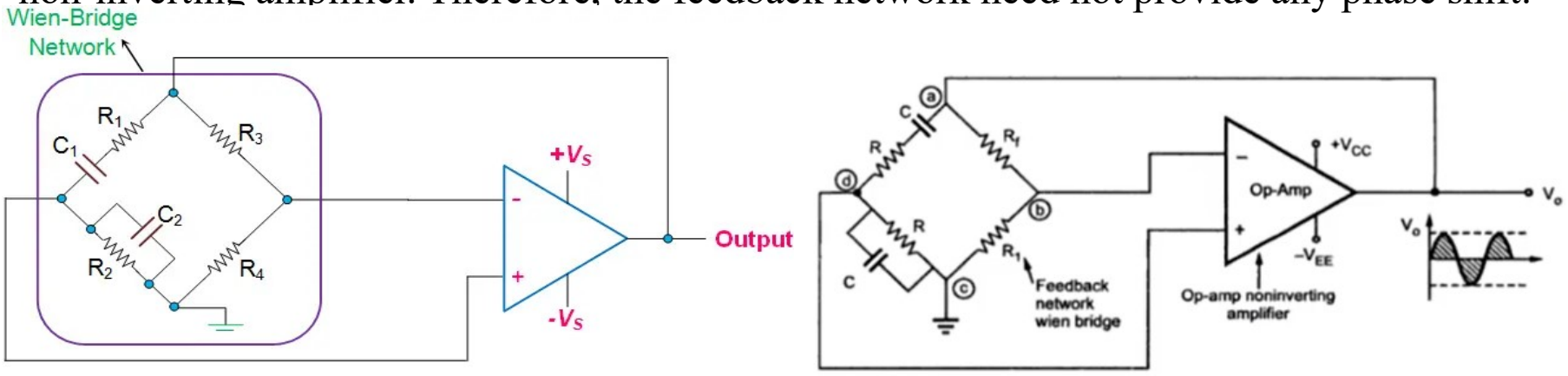


Figure 3 Wien-Bridge Oscillator Using an Op-Amp

- The two arms of the bridge namely R_1C_1 in series and R_2 C_2 in parallel are called frequency sensitive arms.
- The type of feedback is called lead-lag network.
- The gain of the non inverting amplifier can be adjusted using the resistor R_f and R_1.

$$A = 1 + \frac{R_f}{R_1}$$

- To satisfy the Bharkhausen condition $A\beta \geq 1$. it is necessary that the gain of non inverting amplifier must be min '**3**'.

$$|A| \geq 3 \quad \text{i.e} \quad 1 + \frac{R_f}{R_1} \geq 3$$

$$\frac{R_f}{R_1} \geq 2$$

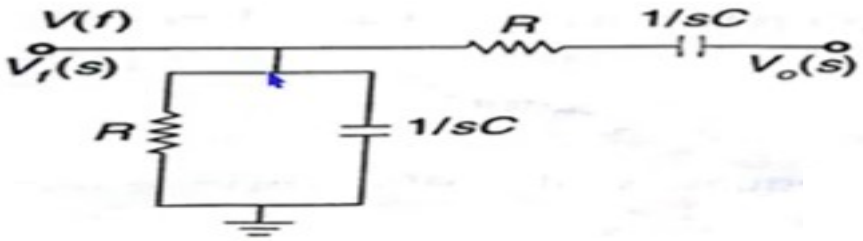
- So the ratio of R_f and R_1 must be ≥ 2.
- The frequency of oscillations is given by,

$$f = \frac{1}{2\pi RC} \text{ Hz}$$

- If the resistors and capacitors used in the bridge are not equal then the frequency of oscillations is given by. $f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$ Hz

- Derivation for frequency of oscillations:

- The equivalent circuit of feedback network is



- If the bridge is balanced.

$$\frac{R_3}{R_4} = \frac{\frac{R_1 + XC_1}{R_2 XC_2}}{R_2 + XC_2}$$ X_{c1} and X_{c2} are the reactance of the capacitors C_1 and C

$$= \frac{R_1 + \left(\frac{1}{j\omega C_1}\right)}{\frac{R_2\left(\frac{1}{j\omega C_2}\right)}{R_2 + \frac{1}{j\omega C_2}}} = \frac{R_1 - j\left(\frac{1}{\omega C_1}\right)}{\frac{R_2\left(\frac{-j}{\omega C_2}\right)}{R_2 - \frac{j}{\omega C_2}}}$$

$$= \frac{\frac{\omega C_1 R_1 - j}{\omega C_1}}{\frac{-R_2 j}{\frac{\omega C_2 R_2 - j}{\omega C_2}}} = \frac{\frac{\omega C_1 R_1 - j}{\omega C_1}}{\frac{-R_2 j}{\omega C_2 R_2 - j}}$$

Contd..

$$= \frac{\omega c_1 R_1 - j}{\omega c_1} \chi \frac{\omega c_1 R_1 - j}{-R_2 j}$$

$$= \frac{\omega c_1 R_1 \omega c_2 R_2 - j\omega c_1 R_1 - j\omega c_2 R_2 - 1}{-j\omega c_1 R_2}$$

$$= \frac{j[\omega c_1 R_1 \omega c_2 R_2 - j\omega c_1 R_1 - j\omega c_2 R_2 - 1]}{\omega c_1 R_1}$$

$$= \frac{j\omega c_1 R_1 \omega c_2 R_2 + \omega c_1 R_1 + \omega c_2 R_2 - j}{\omega c_1 R_2}$$

$$= \frac{\omega c_1 R_1 + \omega c_2 R_2 + j[\omega^2 R_1 R_2 c_1 c_2 - 1]}{\omega c_1 R_2}$$

To get the frequency of the oscillation imaginary part on both the sides made equal to zero

Contd..

$$\omega^2 R_1 R_2 c_1 c_2 - 1 = 0$$

$$\omega^2 R_1 R_2 c_1 c_2 = 1$$

$$\omega^2 = \frac{1}{R_1 R_2 c_1 c_2}$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

If $R_1 = R_2 = R$ and $c_1 = c_2 = c$ then

$$\boxed{f_0 = \frac{1}{2\pi RC}}$$

From the equivalent circuit of Wien bridge oscillator,

$$V_f(s) = V_0(s) \cdot \frac{R \| \frac{1}{SC}}{R + \frac{1}{SC} + R \| \frac{1}{SC}}$$

$$= V_0(s) \cdot \frac{\frac{R}{1+SRC}}{R + \frac{1}{SC} + \frac{R}{1+SRC}}$$

$$= V_0(s) \frac{SRC}{S^2R^2C^2 + 3SRC + 1}$$

Therefore, feedback factor is

$$\beta = \frac{V_f(s)}{V_0(s)} = \frac{SRC}{S^2R^2C^2 + 3SRC + 1}$$

We know that $A\beta = 1 \rightarrow A = \frac{1}{\beta} = \frac{S^2R^2C^2 + 3SRC + 1}{SRC}$

Substitute $S = j\omega_0$ to the above equation

We know that $\omega_0 = \frac{1}{RC} \left[f_0 = \frac{1}{2\pi RC} \right]$

$$A = 3 = \frac{1}{\beta} \qquad \therefore \beta = \frac{1}{3}$$

- **Advantages:**
- Easy to adjust frequency
- Perfect sine wave oscillator
- Best audio frequency oscillations

Problem:

- Design a wien bridge oscillator for f_0 = 10 kHz

Solution : Choose C = 0.01 μF

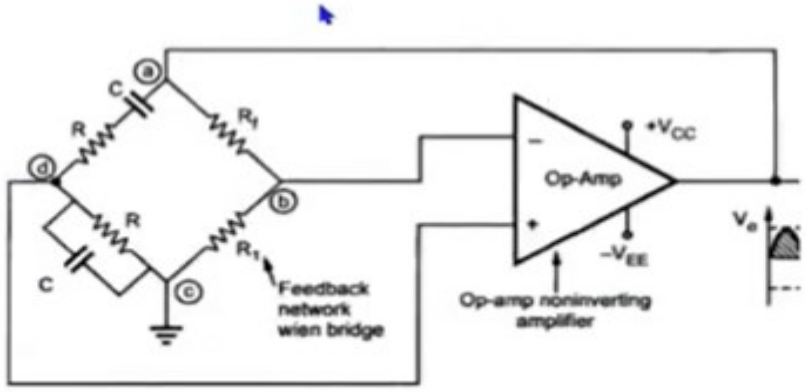
$$R = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 10 \times 10^3 \times 0.01 \times 10^{-6}} = 1.5915\ k\Omega$$

Choose standard value of 1.5 kΩ

$$R_f = 2\,R_1$$

$$R_1 = 1\ k\Omega$$

$$R_f = 2\ k\Omega$$



Problem:

1. Design a phase shift oscillator for the frequency 500Hz with +/-12V supply voltage

Solution : As f is less than 1 kHz, Use op-amp 741 with $I_b(max) = 50$ nA.

$$I_1 = 100\, I_b(max) = 5\ \mu A$$

$$R_f = \frac{V_o(sat)}{I_1} \quad \text{where } V_o(sat) = 12 - 1 = 11\ V$$

$$= \frac{11}{50\times10^{-6}} = 2.2\ M\Omega \text{ (standard value)}$$

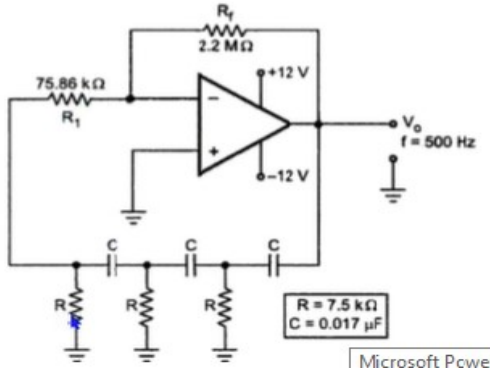
$$A_{CL} = \frac{R_f}{R_1} \geq 29$$

$$R_1 = \frac{R_f}{29} = \frac{220\times10^3}{29} = 75.86\ k\Omega$$

Use standard value of 75.86 kΩ

$$R = \frac{R_1}{10} = \frac{75.8\times10^3}{10} = 7.5\ k\Omega \text{ (standard value)}$$

$$C = \frac{1}{2\pi\sqrt{6}\,f\,R} = \frac{1}{2\pi\sqrt{6}\times500\times7500} = 0.017\ \mu F$$



555 timer:

The **555 Timer** IC got its name from the three 5KΩ resistors that are used in its voltage divider network. This IC is useful for generating accurate time delays and oscillations (accurately produce the required output waveform).

It can give time delays for microseconds to hours.

It can work in a supply range +5V to +18V and can drive loads up to 200mA.

It can be designed with TTL and CMOS logic circuits.

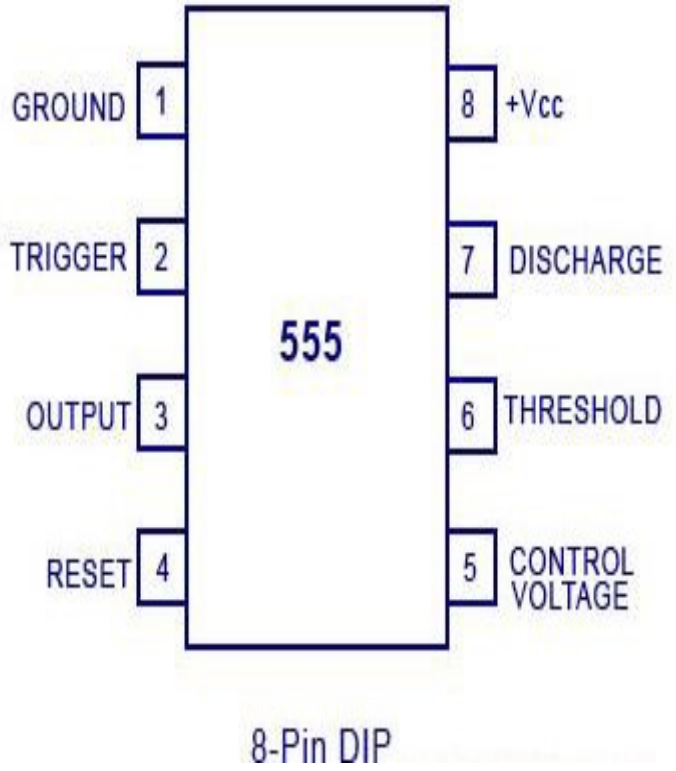
The 555 timer IC was introduced in the year 1970 by Signetic Corporation and gave the name **SE/NE 555 timer.**

It is one of the monolithic (**a complete circuit or group of circuits manufactured in a single piece of silicon)** timing circuits and important use of this IC is providing accurate and constant delay to the circuit. And the other advantages of this IC are very compact size, more reliable, and low cost also.

APPLICATIONS OF 555IC:

1.Monostable multivibrator
2. Astable multivibrator,
3. Schmitt trigger
4. Dc-DC converters
5. Waveform generators
6. Voltage Monitor
7. Traffic light control
8. Temperature measurement and etc.,

PIN DIAGRAM OF IC 555



8-Pin DIP

Temperature Range:

SE555: -55^0C to 125^0C

NE555: 0 to 70^0C

- Available in 3 types of packages
  - — 8-pin Metal can package
  - — 8-pin DIP (NE/SE 555 & TLC 555)
  - — 14-pin DIP Package (Consist of two 555 timers)
- Good temperature stability.
- Widely available in market and less cost like op-amp .

Pin descripion:

Pin 1: Grounded Terminal: The given input voltages and output voltages are measured with respect to ground.

Pin 2: Trigger Terminal: The trigger voltage defines the output of the timer.

Pin 3: Output Terminal: Output of the timer is available at this pin. There are two ways in which a load can be connected to the output terminal. One way is to connect between output pin (pin 3) and ground pin (pin 1) or between pin 3 and supply pin (pin 8). The load connected between output and ground supply pin is called the normally on load and that connected between output and ground pin is called the normally off load.

Pin 4: Reset Terminal: It is used to reset the timer .By applying high signal to the terminal it can reset the timer.

Pin 5: Control Voltage Terminal: The amount of control voltage controls the width of the output pulses.

Pin 6: Threshold Terminal: This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of 2/3 VCC. If the applied voltage crosses the threshold level then the upper comparator output becomes high and the output goes to low.

Pin 7 : Discharge Terminal: This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. When the transistor is cut-off, the capacitor charges at a rate determined by the external resistor and capacitor.

Pin 8: Supply Terminal: the supply voltage range of the IC can be +5v to +18v.

FUNCTIONAL BLOCK DIAGRAM OF 555 TIMER

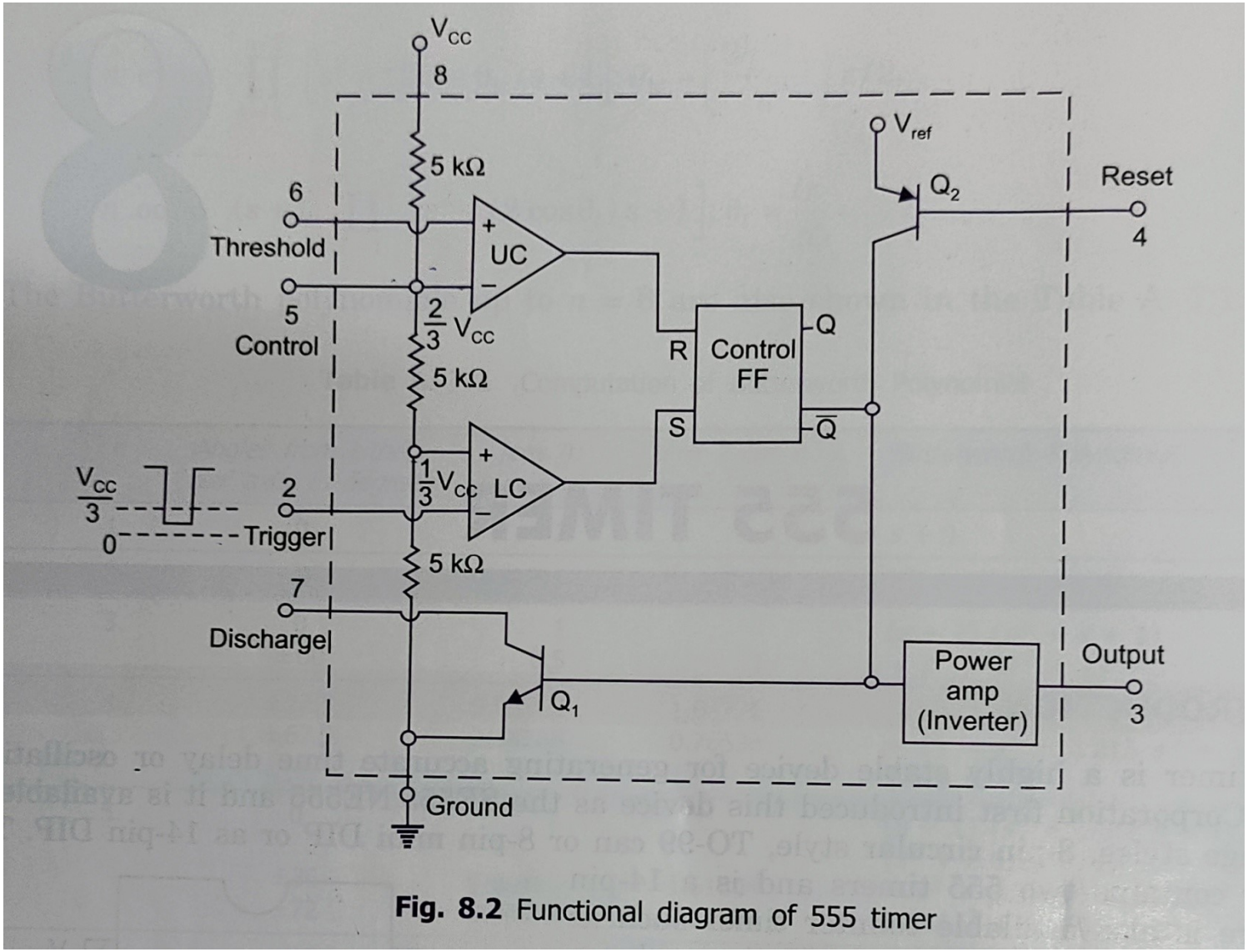
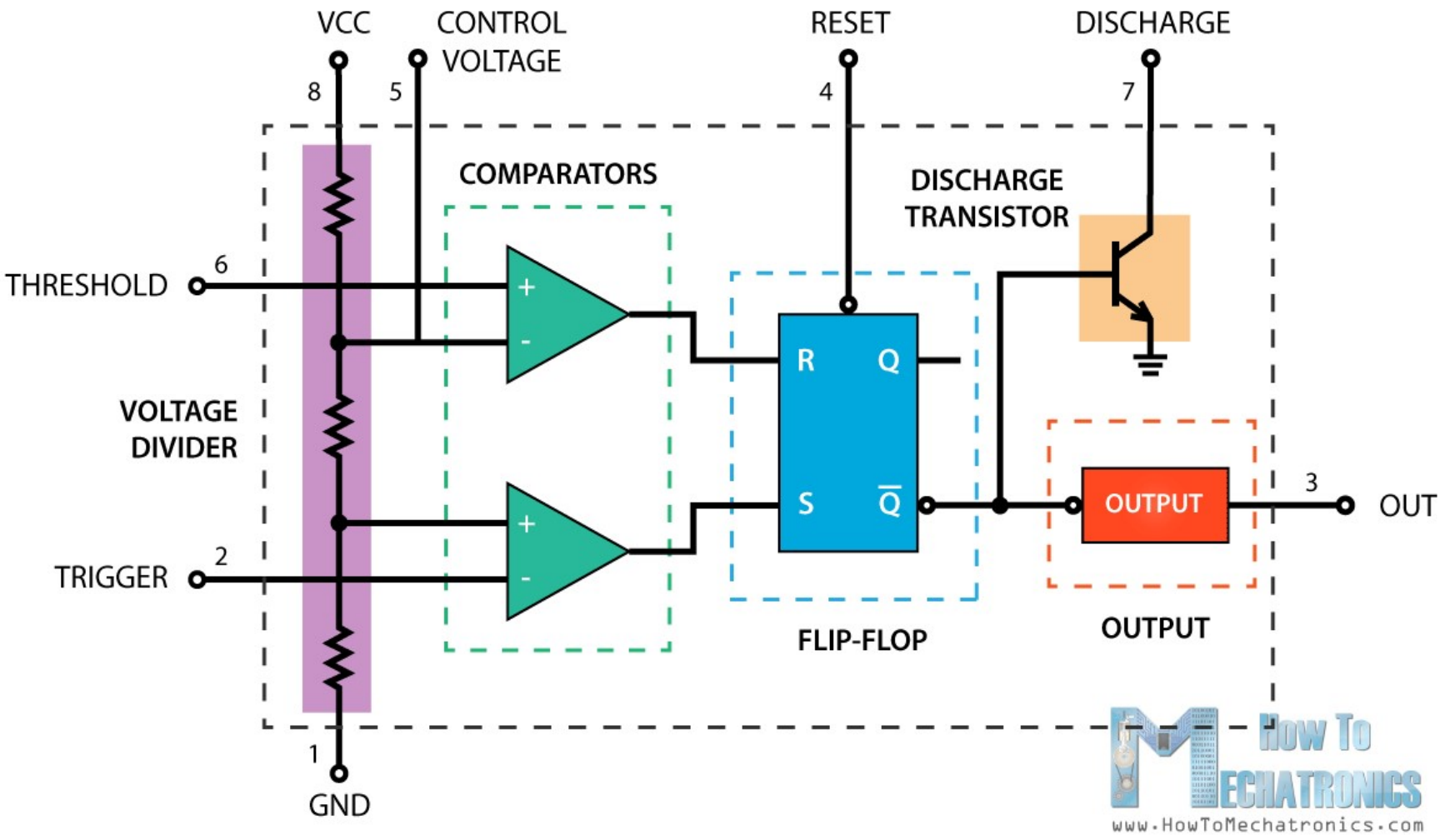


Fig. 8.2 Functional diagram of 555 timer

555 Timer Block Diagram



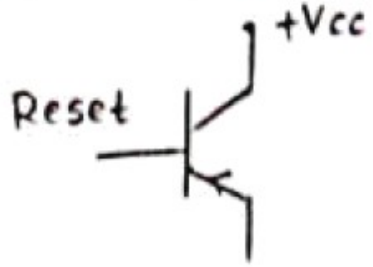
WORKING PRINCIPLE

The above block diagram consists of upper and lower comparators , flip flops, invertors ,amplifier and resistive network.

The resistive network connected here are act as a voltage divider which divides the Vcc into 2 levels, one level is 2/3Vcc and one more level is 1/3Vcc.
2/3 Vcc is given to the inverting terminal of upper comparator it is it‟s threshold level and (1/3)Vcc at the noninverting terminal of the lower comparator.
The upper and lower comparator are used to set and reset the flip flop and also these 2 comparators are the responsible for charging and discharging the transistor Q1 and Q2 .
The upper comparator has the reference level of 2/3 Vcc and the lower comparator has the reference level of 1/3Vcc.In general the threshold voltage and trigger voltage can control the timer , so there is no need of special control voltage given to it.

If we want to change the width of the pulse, we have to give control voltage separately at pin 5.

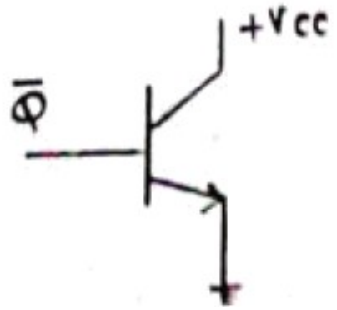
- PNP Transistor : Q_1



If Reset = 0 Q_1 is ON

= 1 Q_1 is OFF

- NPN Transistor : Q_2



If $\bar{Q} = 0$, Q_2 is OFF

= 1, Q_2 is ON

- **Comparator - 1 : C1**

This compares input voltages threshold and $\frac{2}{3}V_{cc}$ Output is R. So,

$$R = \begin{cases} 1 & \text{Threshold} > \frac{2}{3}V_{cc} \\ 0 & \text{Threshold} < \frac{2}{3}V_{cc} \end{cases}$$

- **Comparator 2 : C2**

This compares input voltages $\frac{1}{3}V_{cc}$ and trigger. Output is S. So,

$$S = \begin{cases} 1 & \frac{1}{3}V_{cc} > \text{trigger} \\ 0 & \frac{1}{3}V_{cc} < \text{trigger} \end{cases}$$

- **Flip Flop**

S	R	Q_n	$\bar{Q}_n$
0	0	Prev	Prev
0	1	0	1
1	0	1	0
1	1	—	—

- In 555 timer, output is connected to $\bar{Q}$ of SR flip flop through inverter. So,

O/p : Q

MONOSTABLE MULTIVIBRATOR : Monostable Multivibrator is also known as One Shot Multivibrator. As its name indicates it has one stable state and it switches to unstable state for a predetermined time period T when it is triggered. The time period T is determined by the RC time constant in the circuit. Monostable mode of 555 Timer is commonly used for generating Pulse Width Modulated (PWM) waves.

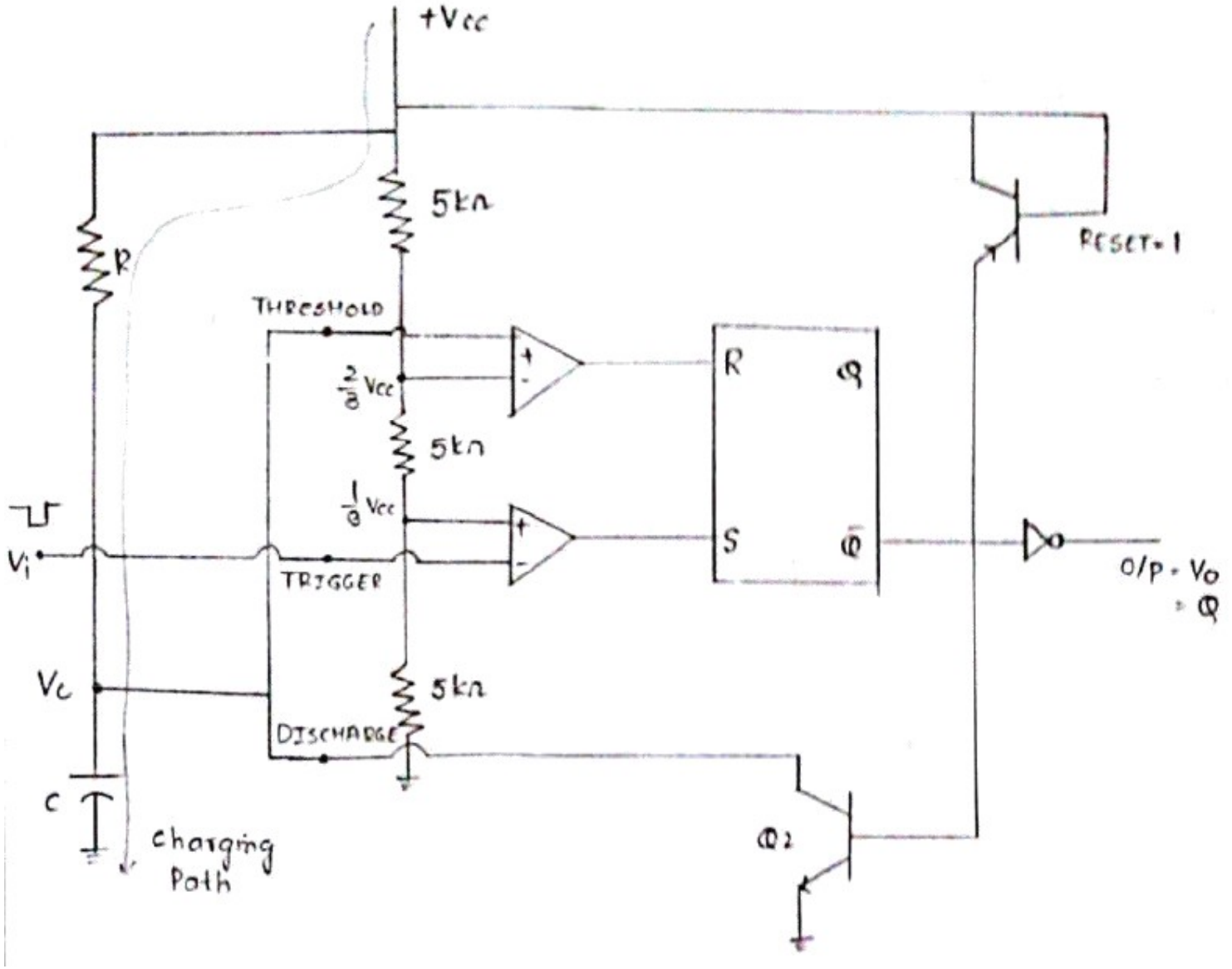
A monostable multivibrator, often called a one-shot multivibrator, is a pulse- generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer.

In a stable or standby state the output of the circuit is approximately zero or at logic- low level.

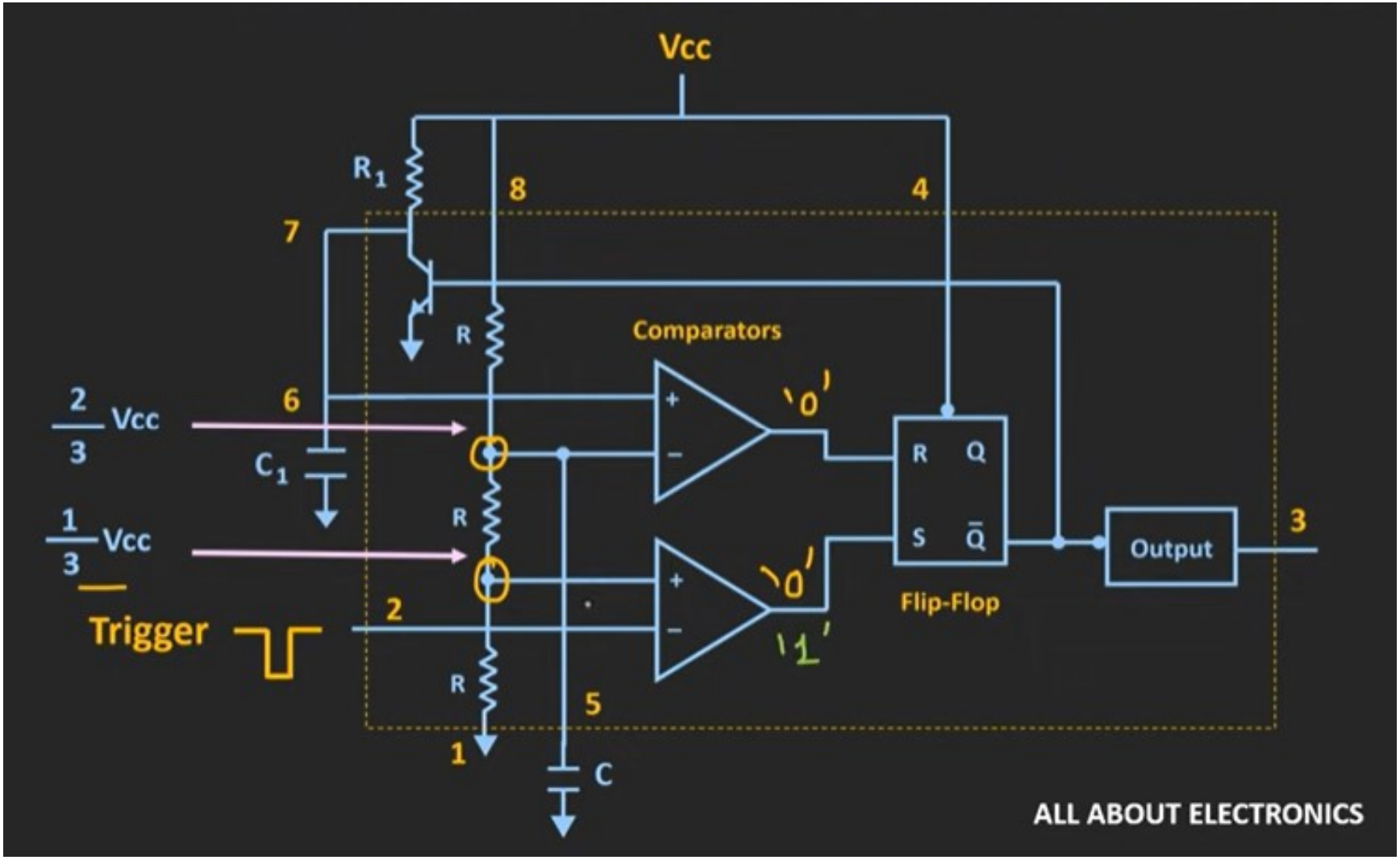
When an external trigger pulse is applied, the output is forced to go high (≈VCC). The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied.

Then the cycle repeats. The monostable circuit has only one stable state (output low), hence the name mono- stable. Normally, the output of the mono- stable multivibrator is low.

MONOSTABLE MULTIVIBRATOR



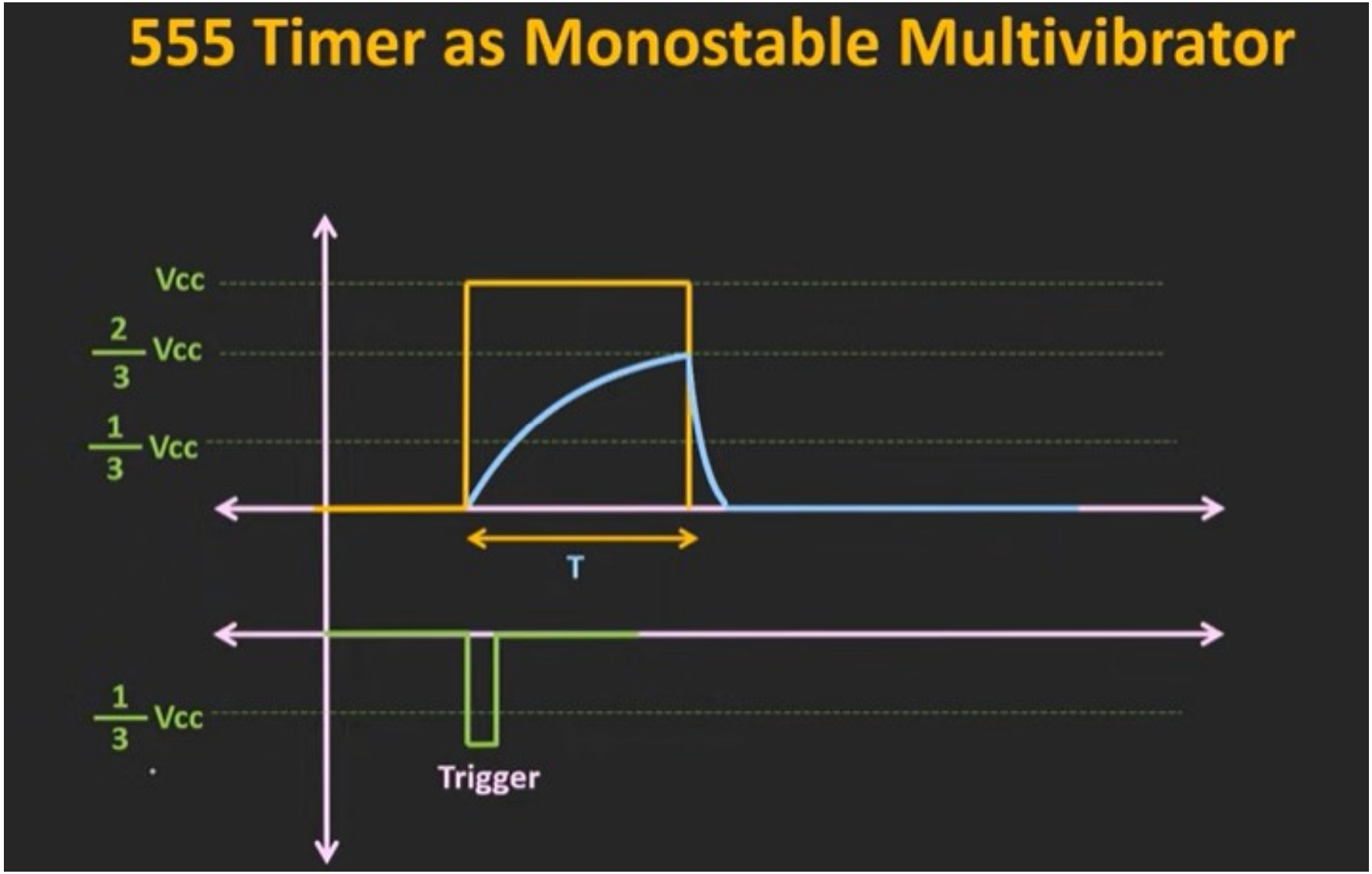
MONOSTABLE MULTIVIBRATOR



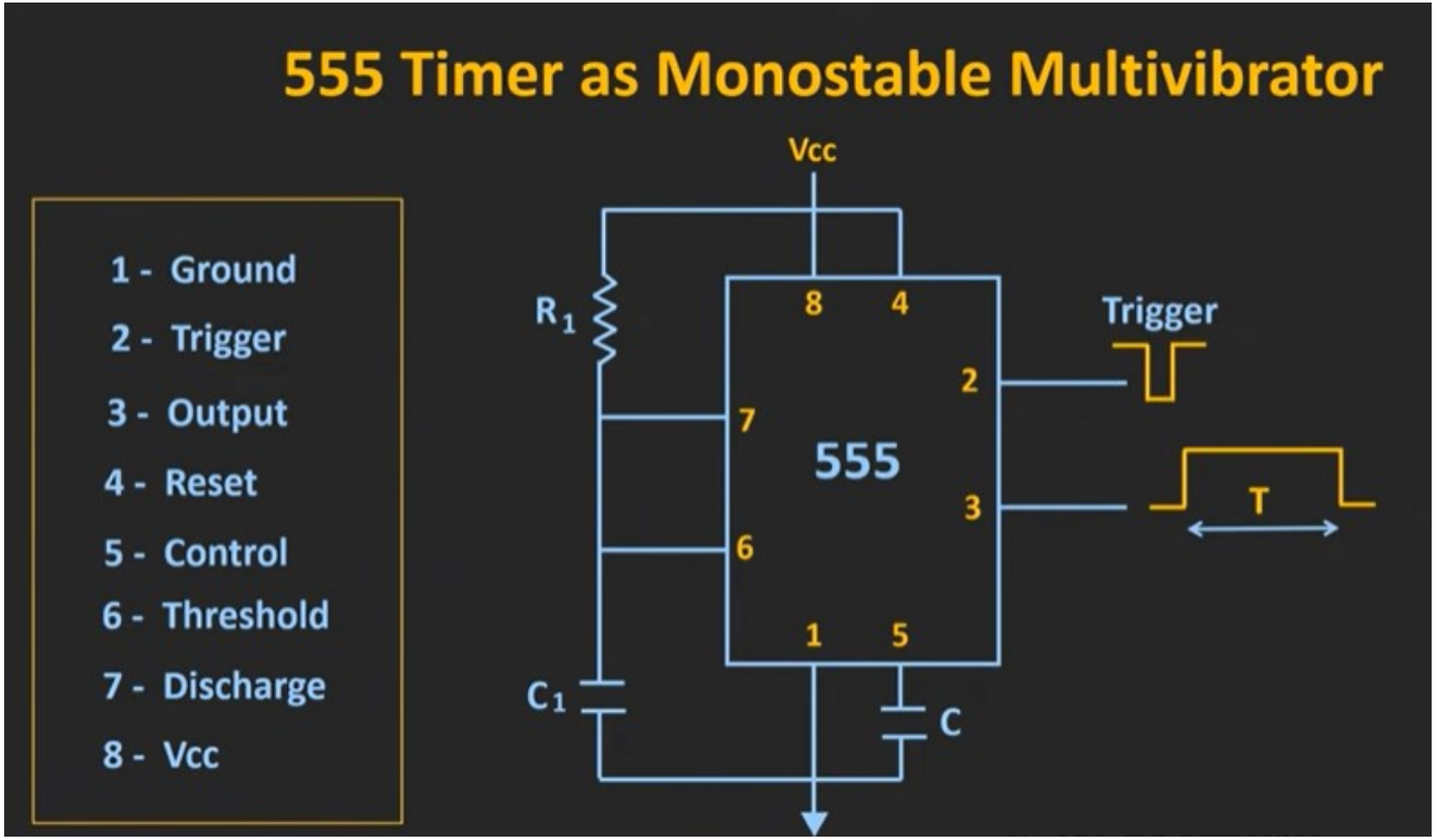
MONOSTABLE MULTIVIBRATOR

- The Monostable Multivibrator will be in its stable state (Output LOW) until it is triggered.
- When a negative trigger is applied to the Trigger pin of 555 Timer, output of lower comparator will become HIGH and output of upper comparator will be LOW, since the capacitor voltage is zero. This makes the output HIGH.
- The Discharge transistor turns OFF and the capacitor starts charges through resistor R to Vcc.
- After the negative trigger, output of lower comparator becomes LOW and that of upper comparator remains LOW. Since both inputs of the SR Flip Flop are LOW, output will not change, so the output is HIGH.
- When the capacitor voltage will become greater than 2/3 Vcc, output of upper comparator becomes HIGH and that of lower comparator remains LOW, so the output becomes LOW.
- This turns ON the discharge transistor and the capacitor discharges.
- The circuit remains in its stable state (Output LOW) until next trigger occurs.

555 Timer as Monostable Multivibrator

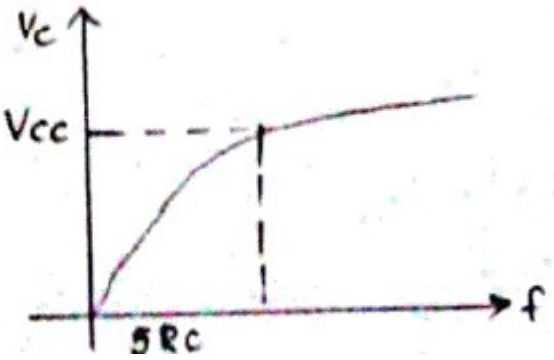


555 Timer as Monostable Multivibrator



- In this,
  Capacitor voltage is connected to threshold and discharge terminals.
- A negative pulse of limited time period (very less) is applied as input to the trigger input

- Initially,
  Capacitor will charge upto maximum applied voltage Vcc in exponential path.
  After 5 time constants [5RC seconds], Vc will be equal to Vcc



Operation:

Let consider the output of the flip flop is low then he circuit is in stable state. If we are giving negative pulse to the comparator2 means the output of the comparator goes high when the trigger voltage falls to 1/3Vcc and it will reset the flip flop. So the transistor goes to off state, then the output of the flip flop goes high. This is called the transition of the output from stable to quasi-stable state, as shown in figure.

As the discharge transistor is cutoff, the capacitor C begins charging toward +VCC through resistance RA with a time constant equal to RAC. When the increasing capacitor voltage becomes slightly greater than +2/3 VCC, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low. the RC time constant controls the width of the output pulse. The time during which the timer output remains high is given as

- Initially, $V_c = 0$ and Trigger $= V_{cc}$

So,

$V_c < \frac{2}{3}V_{cc}$ So, R = 1 Output = 0 [LOW]

Trig $> \frac{1}{3}V_{cc}$ So, S = 0

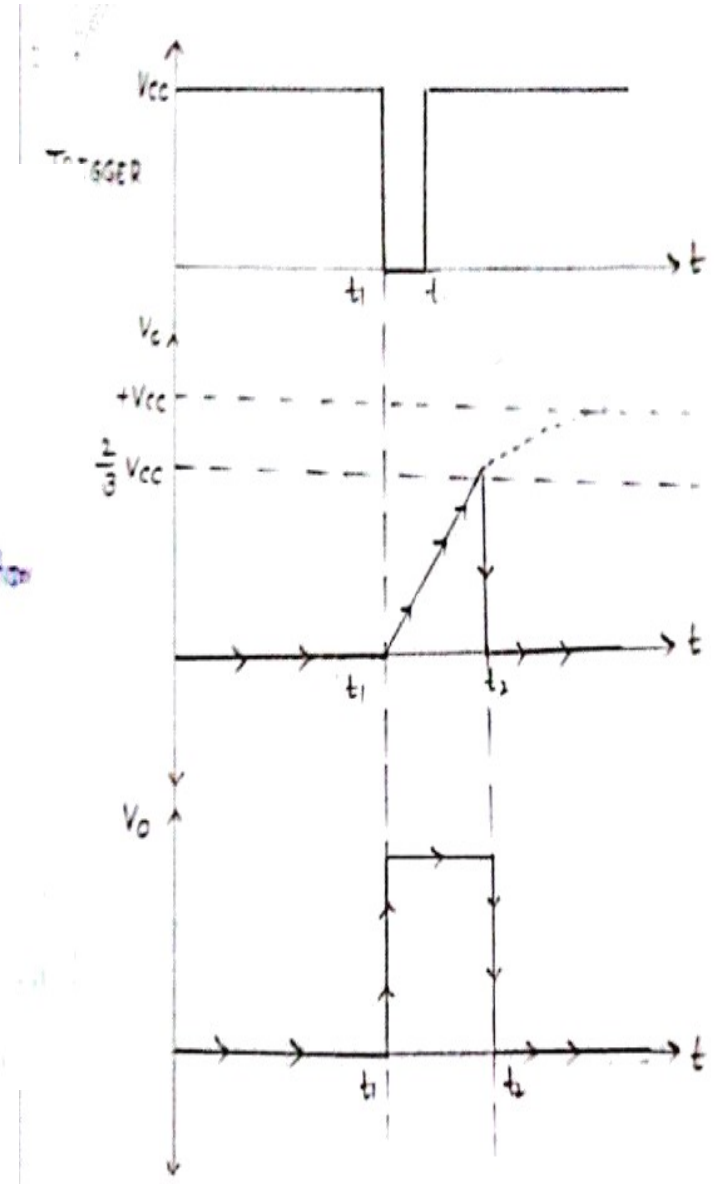
Output $\Phi = 0$, so $\bar{\Phi} = 1$ [HIGH] then Q2 will be ON, i.e. capacitor terminal is connected to ground. So, $V_c = 0$

- But, at $t = t_1$, trigger is pressed, i.e, -ve pulse.

So, trigger = 0

$V_c < \frac{2}{3}V_{cc}$ R = 0 Output = 1 [HIGH]

Trig $< \frac{1}{3}V_{cc}$ S = 1



$\bar{Q} = 0$, so Q2 transistor is OFF. ,i.e, capacitor is connected to V_{cc} through resistor so it tries to charge upto V_{cc}

But at $t = t_2$,

Capacitor charges upto $\frac{2}{3} V_{cc}$. As time increases, it tries to charge more than $\frac{2}{3} V_{cc}$.

So,

$t = t_2+$

$V_c > \frac{2}{3} V_{cc}$ R = 1 output = 0 [LOW]

trigger = V_{cc} S = 0

$> \frac{1}{3} V_{cc}$

As $\bar{Q} = 1$, capacitor is connected to ground. So, V_c becomes zero within short period.

After $t = t_2$, output will be zero and V_c will be zero until the next trigger is applied.

If applied, then again one pulse exists at the output

PULSE TIME CALCULATION:

from t_1 to t_2, pulse is ON. In this duration, capacitor is trying to charge from zero to V_{cc} but at $t = t_2$, $V_c = \frac{2}{3} V_{cc}$.

Let $t_1 = 0$. $t_2 - t_1$ = Pulse Period = $t_2 = T$

Initial Value = 0, final Value = V_{cc} $\tau = RC$

So,

$$V_c(t) = V_f + [V_i - V_f] e^{-t/\tau}$$

$$V_c(t) = V_{cc} + [0 - V_{cc}] e^{-t/RC}$$

$$= V_{cc} [1 - e^{-t/RC}]$$

At $t = t_2$,

$$V_c(t_2) = \frac{2}{3} V_{cc} \qquad (\text{We know } t_2 = T)$$

So,

$$\frac{2}{3} V_{cc} = V_{cc} [1 - e^{-t_2/RC}]$$

$$e^{-T/RC} = 1/3$$

$$\boxed{T = RC \ln 3} \qquad \boxed{T = 1.11\, RC}$$

Applications:

i) Missing Pulse detector
ii) Linear Ramp Generator
iii) Frequency divider
iv) PWM

Applications:

(i) Missing Pulse detector
(ii) Linear Ramp Generator
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(iv) PWM

Missing Pulse Detector

Missing pulse detector circuit using 555 timer is shown in Fig. 8.8. Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~ 0.7 V). The output of the timer goes HIGH. The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains HIGH. However, if a pulse misses, the trigger input is high and transistor Q is cut

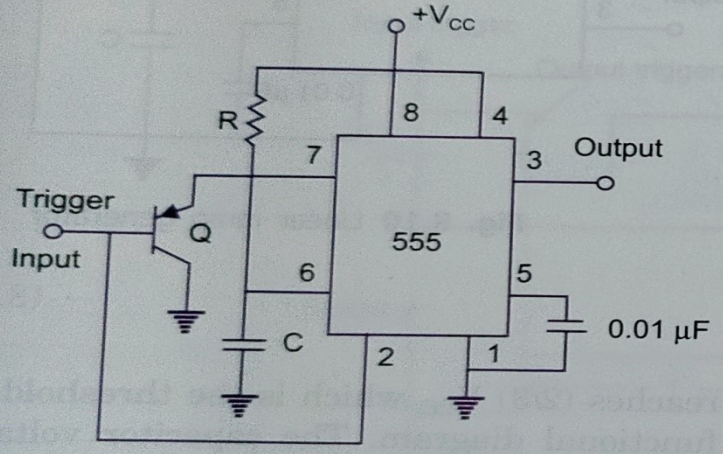


Fig. 8.8 A missing pulse detector monostable circuit

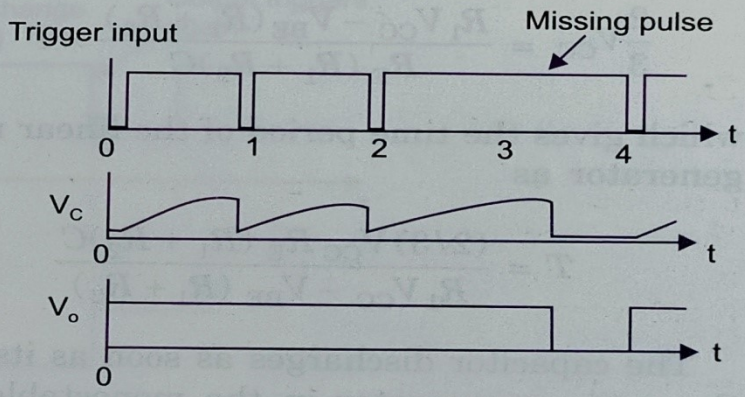


Fig. 8.9 Output of missing pulse detector

Linear Ramp Generator

Linear ramp can be generated by the circuit shown in Fig. 8.10. The resistor R of the monostable circuit is replaced by a constant current source. The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage v_c can be written as

$$v_c = \frac{1}{C}\int_0^t i\,dt \tag{8.3}$$

where i is the current supplied by the constant current source. Further, the KVL equation can be written as

$$\frac{R_1}{R_1 + R_2}\, V_{CC} - V_{BE} = (\beta + 1) I_B R_E \approx \beta I_B R_E = I_C R_E = i R_E \tag{8.4}$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. Therefore,

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)} \tag{8.5}$$

Now putting the value of the current i in Eq. 8.3, we get

$$v_c = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{C\, R_E (R_1 + R_2)} \times t \tag{8.6}$$

At time $t = T$, the capacitor voltage v_c becomes (2/3) V_{CC}. Then we get

$$\frac{2}{3} V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2) C} \times T \tag{8.7}$$

which gives the time period of the linear ramp generator as

$$T = \frac{(2/3) V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE} (R_1 + R_2)} \tag{8.8}$$

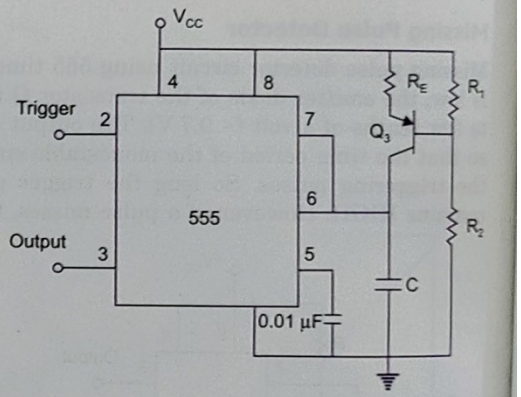


Fig. 8.10 Linear ramp generator

The capacitor discharges as soon as its voltage reaches (2/3) V_{CC} which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The various waveforms are shown in Fig. 8.11.

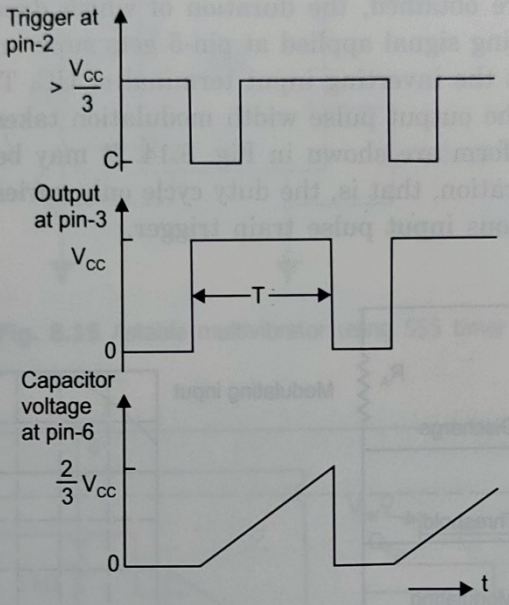


Fig. 8.11 Linear ramp generator output

Frequency Divider

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig. 8.12. The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay. In this way, the output can be made integral fractions of the frequency of the input triggering square wave.

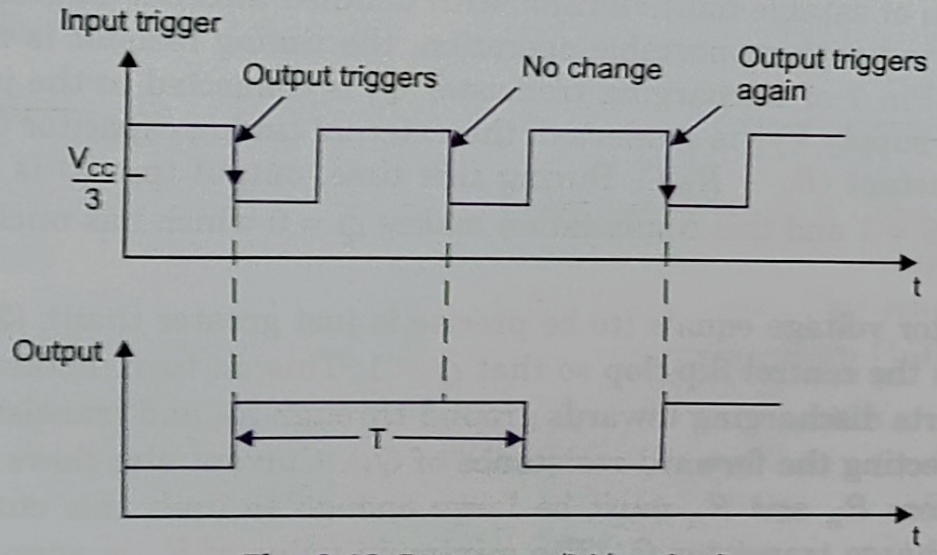


Fig. 8.12 Frequency divider circuit

Pulse Width Modulation

The circuit is shown in Fig. 8.13. This is basically a monostable multivibrator with a modulating input signal applied at pin-5. By the application of continuous trigger at pin-2, a series of output pulses are obtained, the duration of which depends on the modulating input at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) V_{CC} at the inverting input terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig. 8.14. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse train trigger.

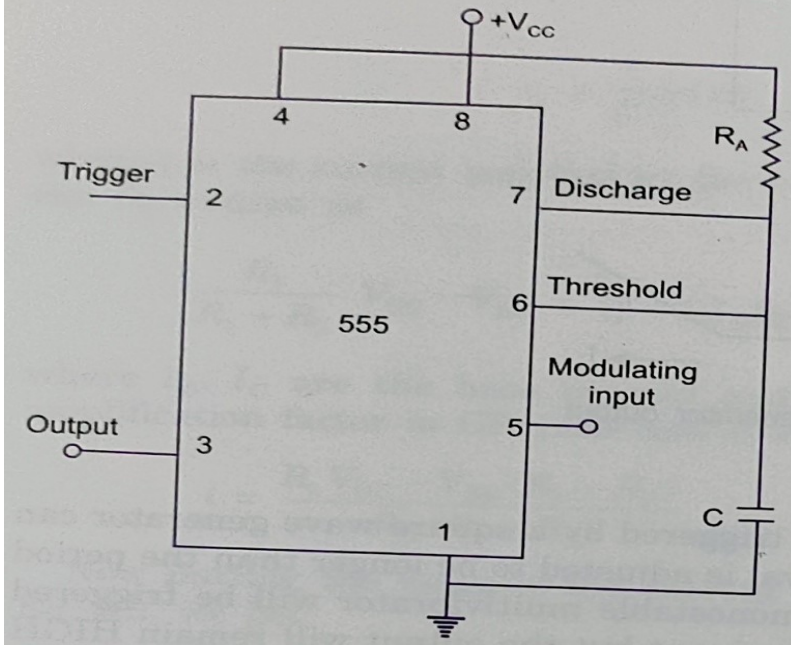


Fig. 8.13 Pulse width modulator

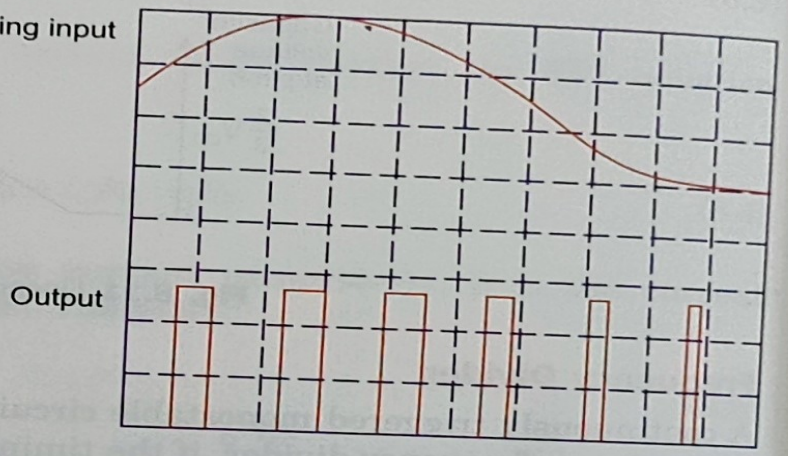


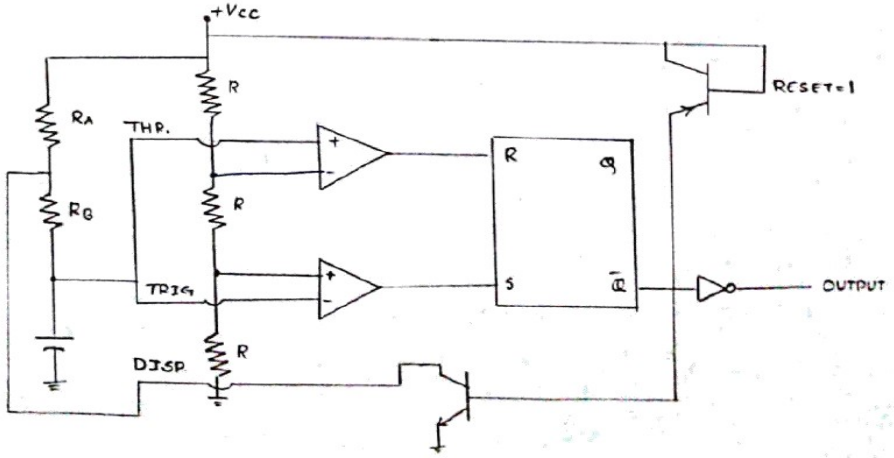
Fig. 8.14 Pulse width modulator waveforms

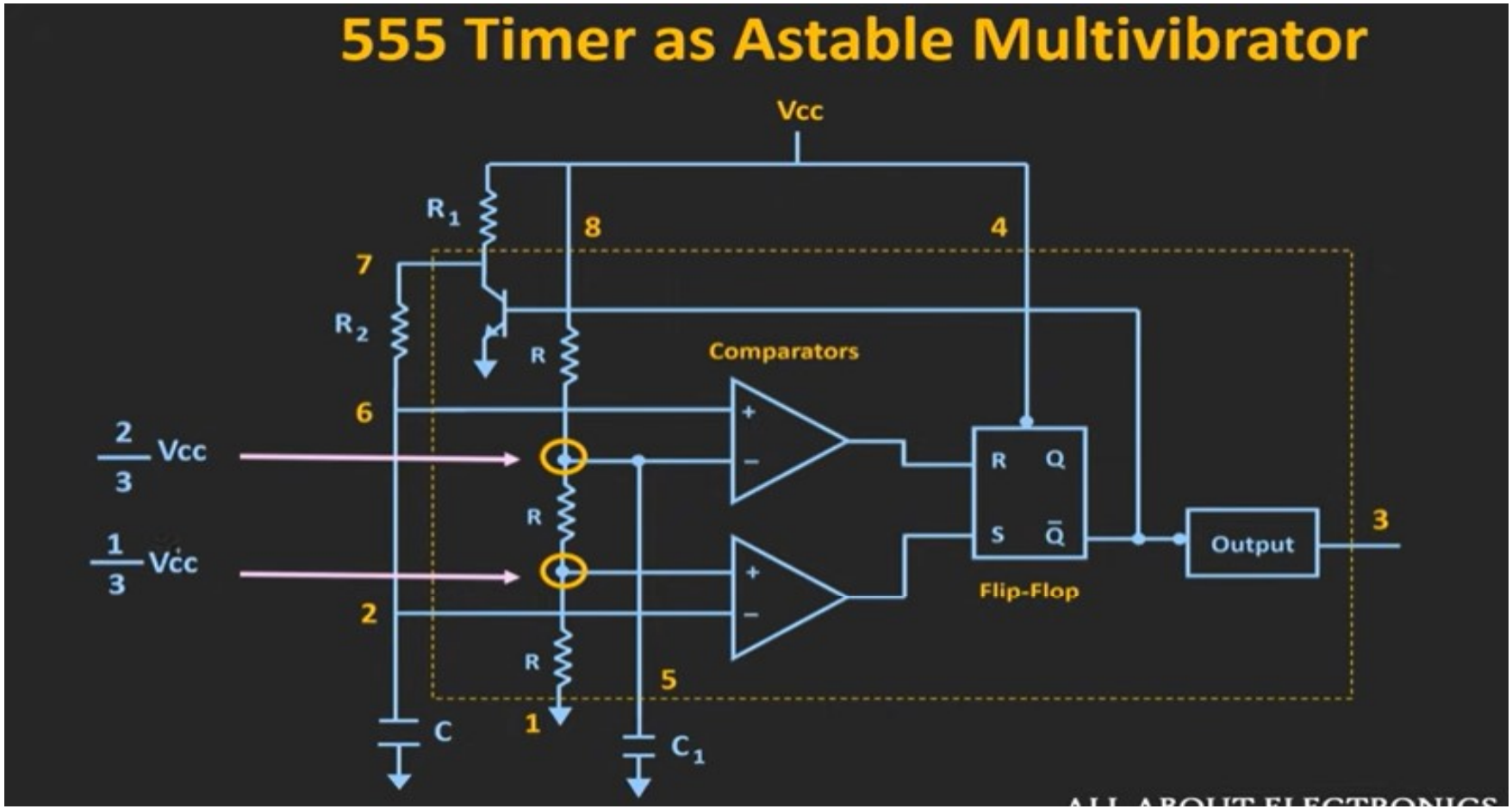
In this modulating signal super imposed to threshold voltage, output voltage change with amplitude of modulating signal.

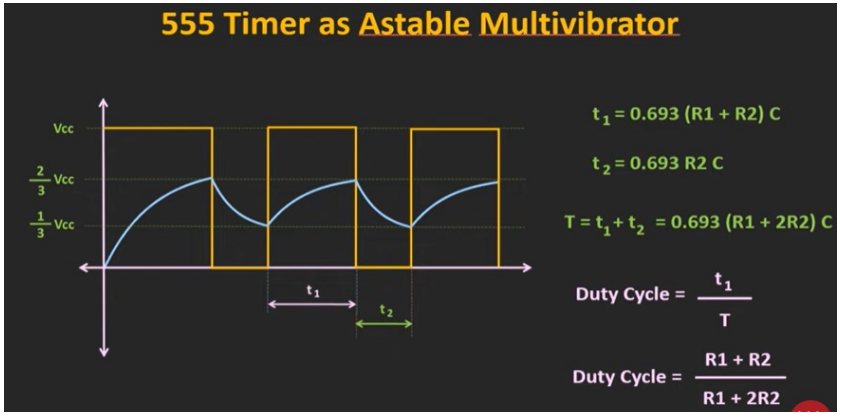
Astable multivibrator:

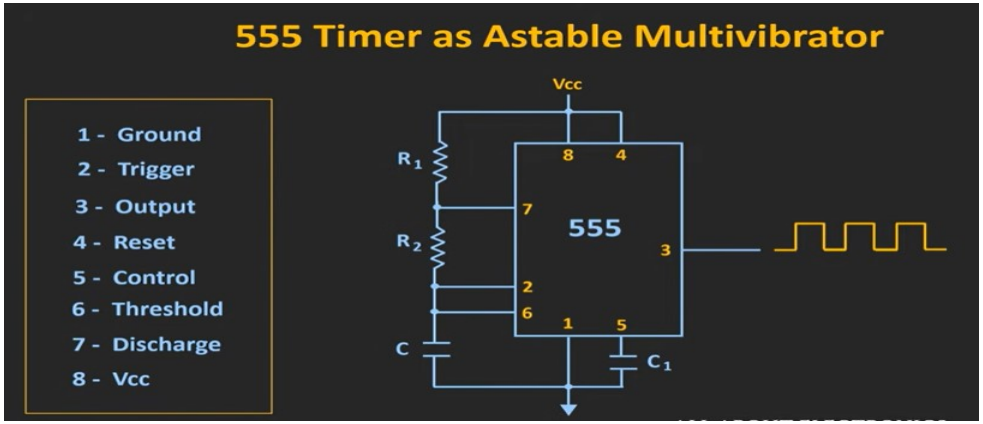
The 555 as an Astable Multivibrator, often called a free-running multivibrator, is a rectangular- wave-generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer. Fig) shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward V through RA and RB. However as soon as voltage across the capacitor equals 2/3 Vcc, comparator I triggers the flip flop, and the output switches low. Now capacitor C starts discharging through RB and transistor Q. **It** is also called as Free Running Multivibrator. It has no stable states and continuously switches between the two states without application of any external trigger. The IC 555 can be made to work as an astable multivibrator with the addition of three external components: two resistors (R_1 and R_2) and a capacitor (C).

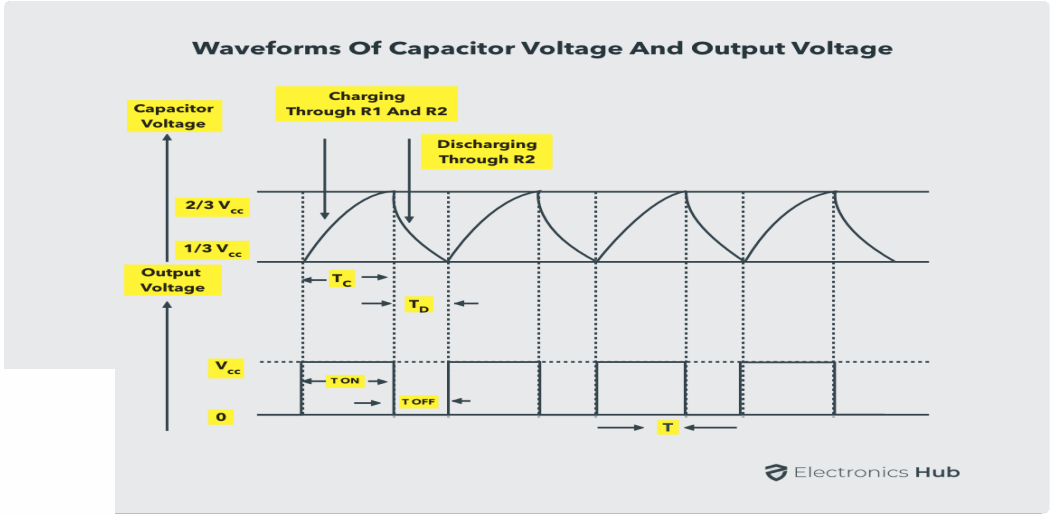
ASTABLE MULTIVIBRATOR:

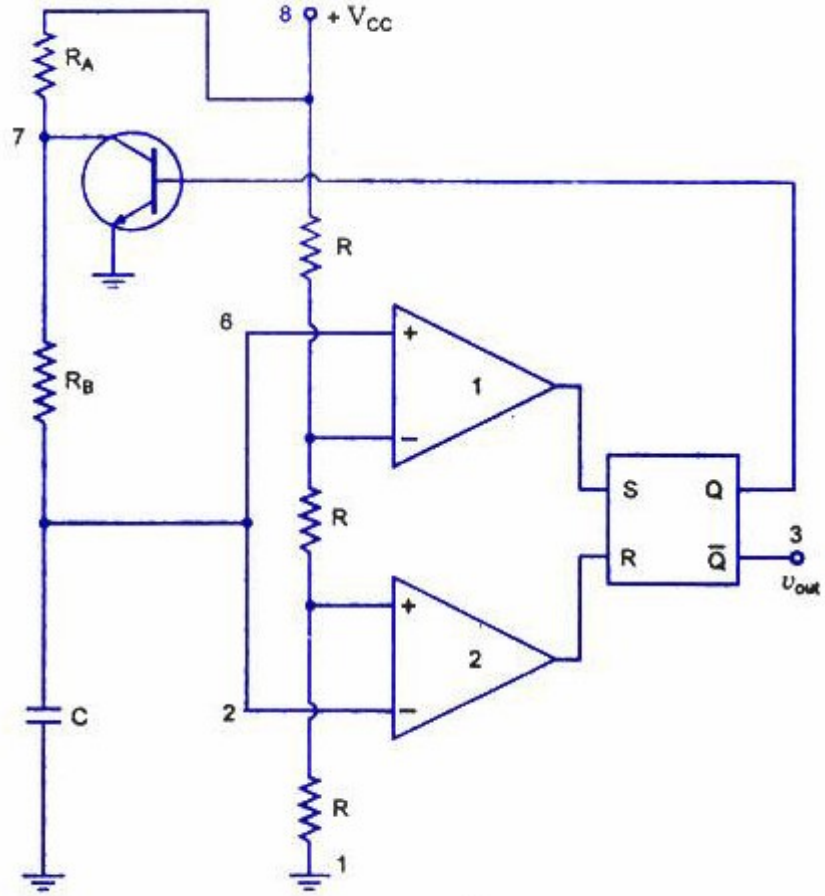



555 Timer as Astable Multivibrator
Vcc
R1
8
4
7
R2
R
Comparators
6
2/3 Vcc
1/3 Vcc
R
R
Q
S
Q̄
Output
3
Flip-Flop
2
R
5
1
C
C1

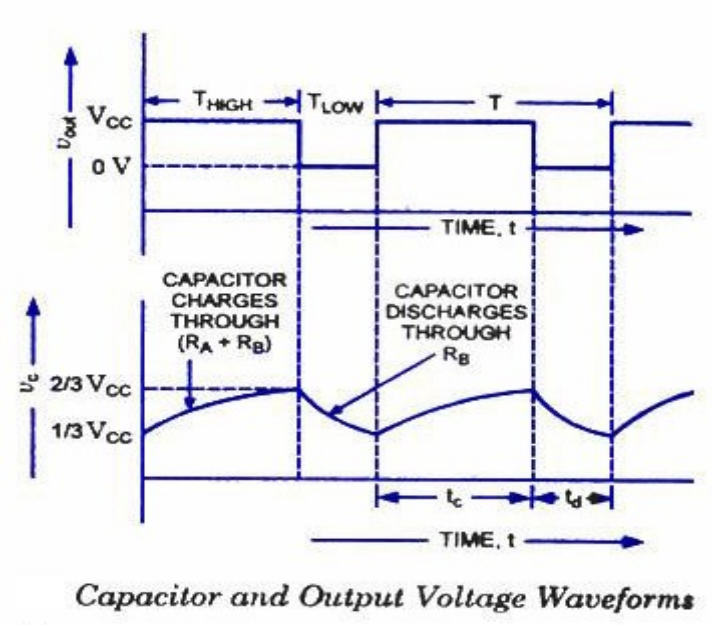

555 Timer as Astable Multivibrator
Vcc
2/3 Vcc
1/3 Vcc
t1
t2
t1 = 0.693 (R1 + R2) C
t2 = 0.693 R2 C
T = t1 + t2 = 0.693 (R1 + 2R2) C
Duty Cycle = t1 / T
Duty Cycle = R1 + R2 / R1 + 2R2


555 Timer as Astable Multivibrator
1 - Ground
2 - Trigger
3 - Output
4 - Reset
5 - Control
6 - Threshold
7 - Discharge
8 - Vcc
Vcc
R1
R2
C
C1
555
8
4
7
3
2
6
1
5





Internal Circuitry With External Connections



Capacitor and Output Voltage Waveforms

Operation:

1. During Interval (0 to t_1) → on time

at $t=0$, $V_c = 0$

$V_2 = 0$ trigger Voltage $< \frac{1}{3} V_{cc}$

o/p of LC is high

SR flf → Reset

$Q = 0$, $\bar{Q} = 1$

↳ T_1 – turn off

as $\bar{Q} = 1$ → o/p → high

o/p remain high till V_c becomes greater than $\frac{2}{3} V_{cc}$

2. During Interval (t_1 for t_2) → off time

as $V_c > \frac{2}{3} V_{cc}$ (at $t = t_1$)

o/p of UC → high

SR flP → set

$Q = 1$, $\bar{Q} = 0$

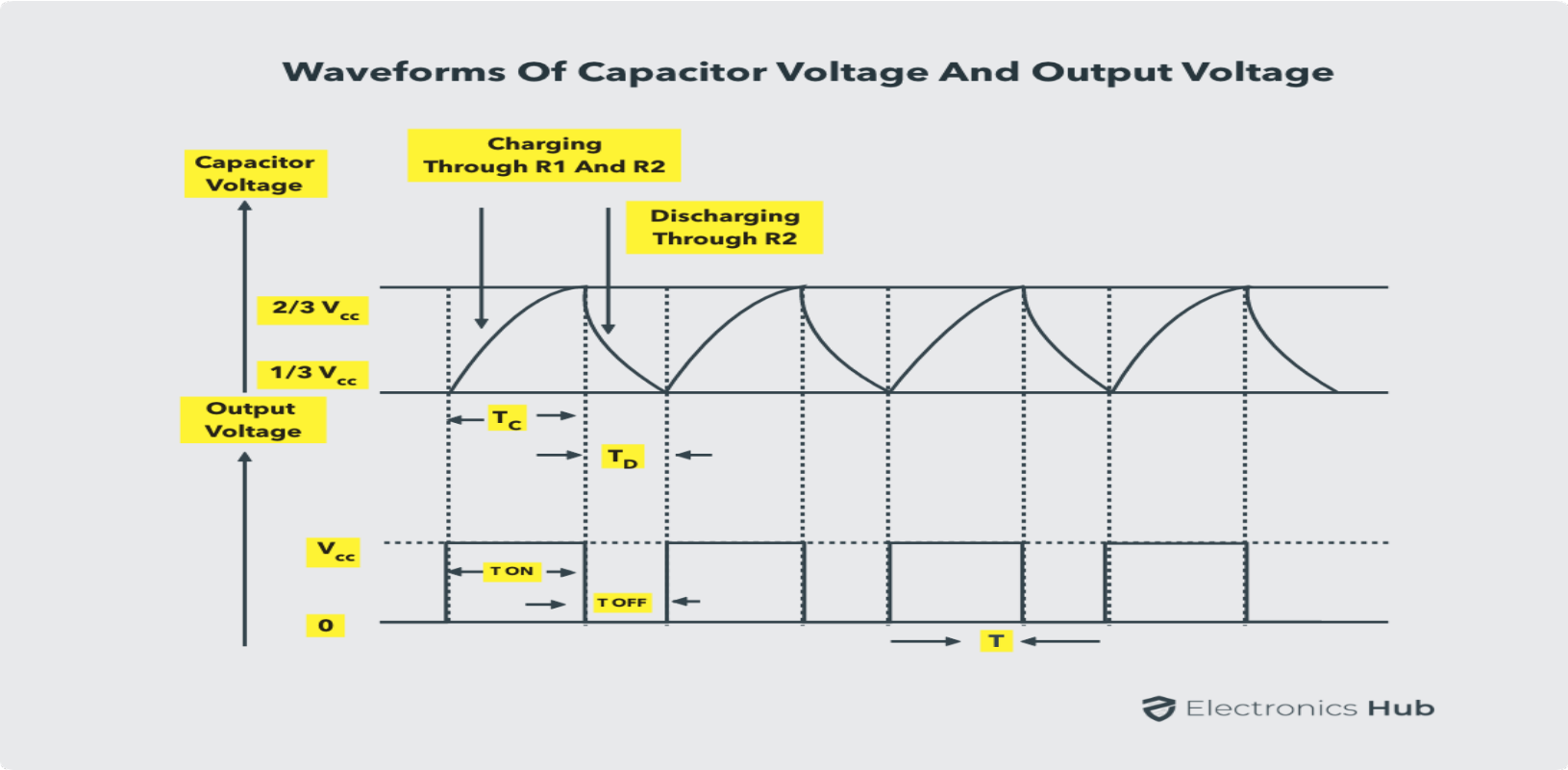
as $Q = 1$, transistor T_1 → turn on

Capacitor discharge through R_B & T_1

at $\bar{Q} = 0$, o/p of multivibrator is → 0

C → discharge till $V_c = \frac{1}{3} V_{cc}$

o/p of LC → high

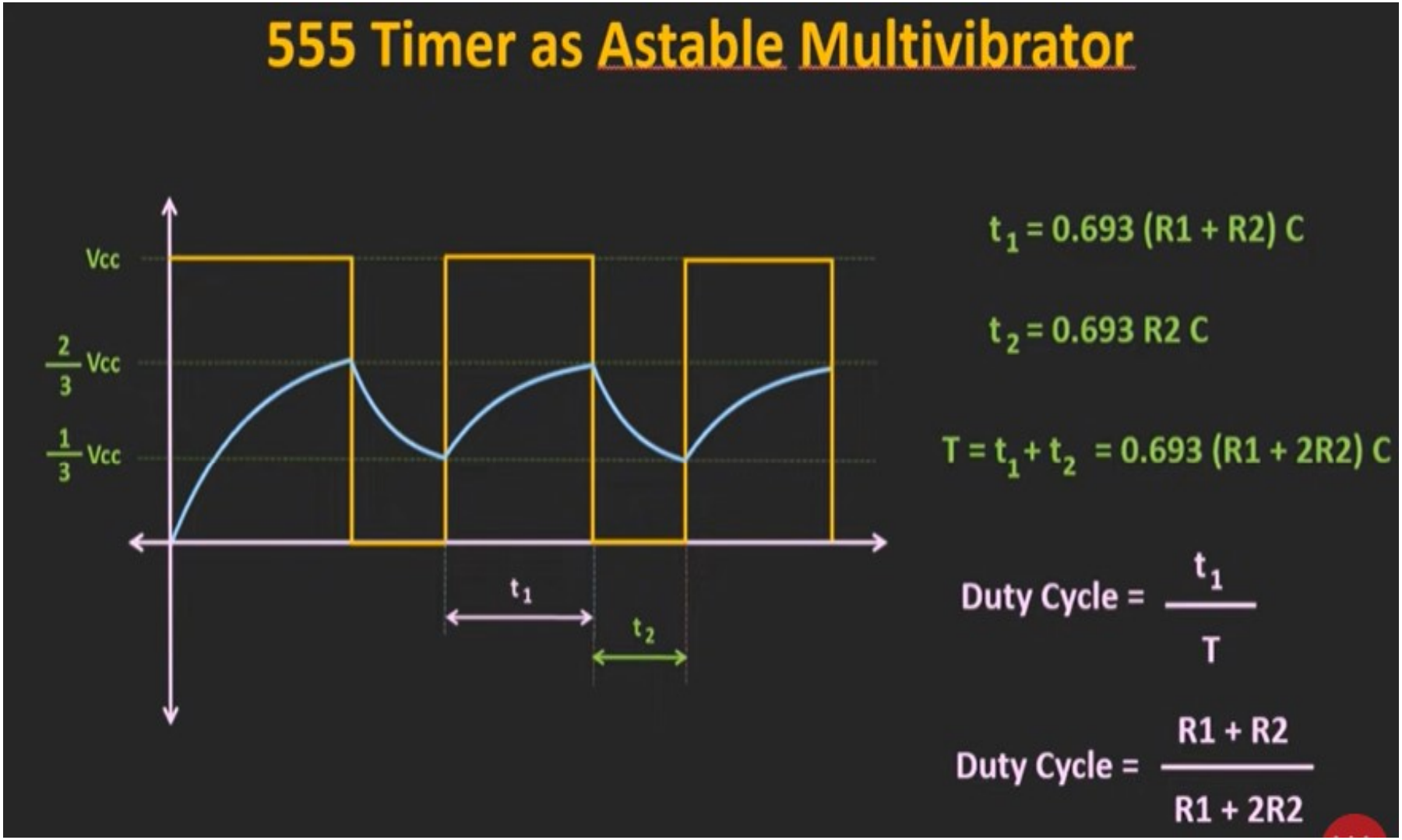


Duty Cycle

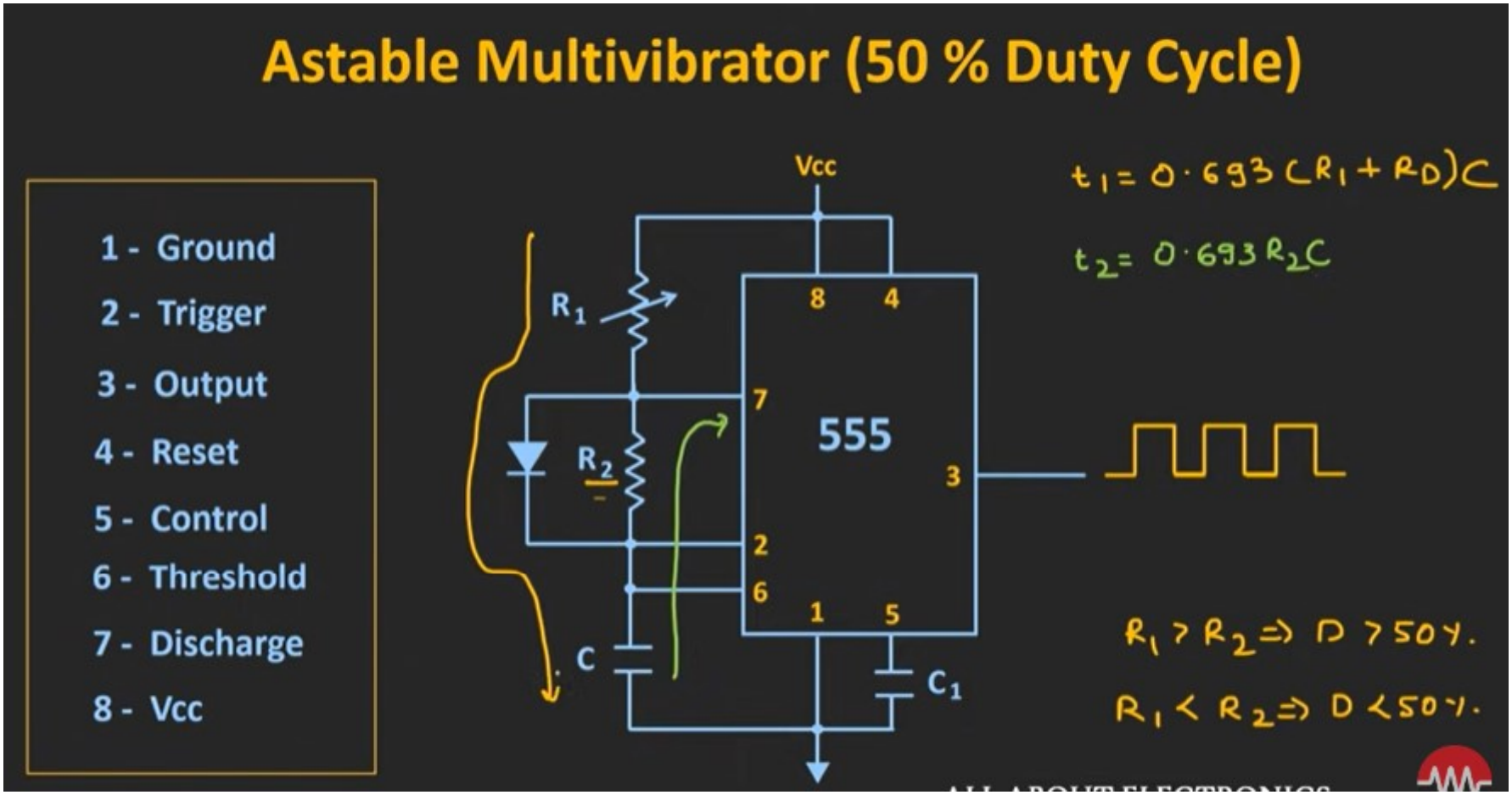
The charging and discharging time constants depends on the values of the resistors R1 and R2. Generally, the charging time constant is more than the discharging time constant. Hence the HIGH output remains longer than the LOW output and therefore the output waveform is not symmetric. Duty cycle is the mathematical parameter that forms a relation between the high output and the low output. Duty Cycle is defined as the ratio of time of HIGH output i.e., the ON time to the total time of a cycle.

$$\text{Duty cycle (D)} = T_{ON} / T$$

T1>T2, the duty cycle is more than 50%.



T1>T2, the duty cycle is more than 50%.



To obtain 50% duty cycle, diode is connected across R2, T1>T2, during the capacitor charging diode is forward bias, charging time of capacitor is $t_1 = 0.693 (R_1 + R_D) C$

during discharging of capacitor, diode reverse bias, capacitor discharge through R2, Discharging time of capacitor is $t_2 = 0.693 R_2 C$

For 50% duty cycle, R1+RD = R2, it is obtain by varying the R1.

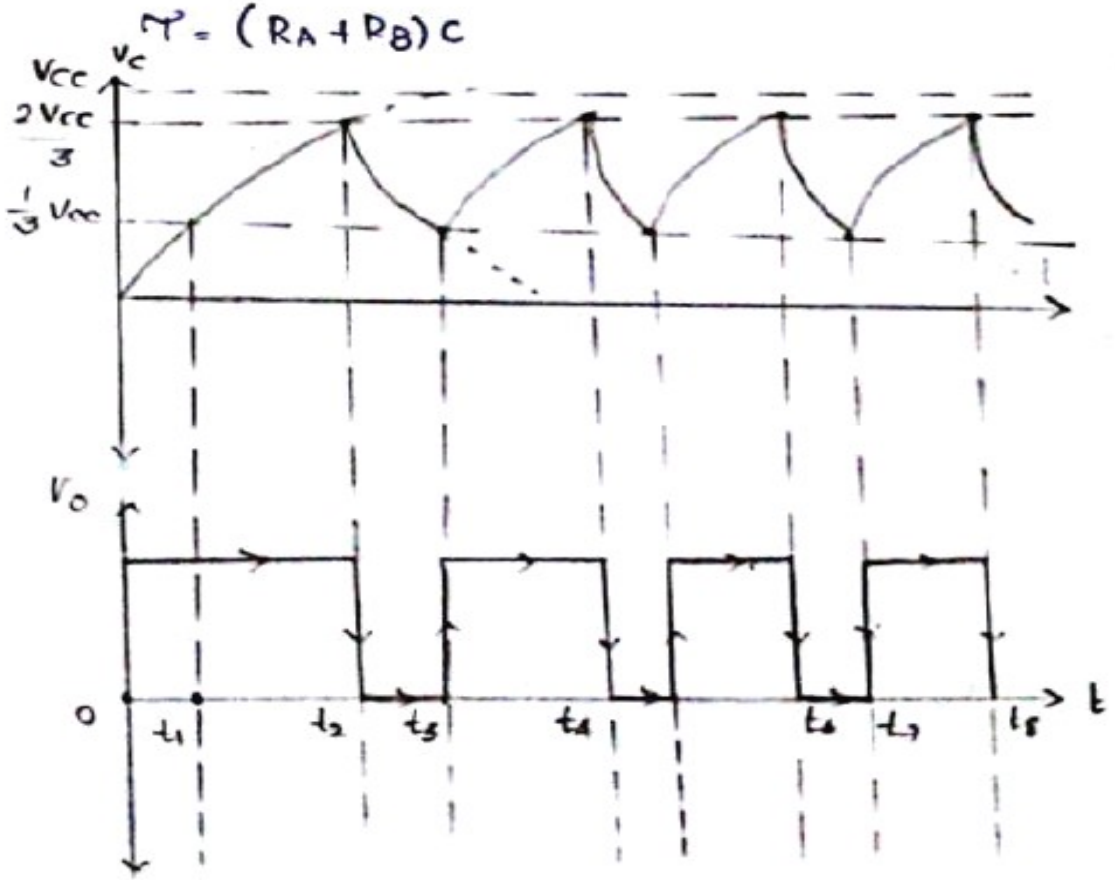
An astable multivibrator is also called as free running multivibrator. In astable multivibrator there is no need of providing trigger to change its states hence the name free running multivibrator or relaxation oscillator.
For explaining the operation of the timer 555 as an astable multivibrator, necessary internal circuitry with external connections are shown in figure.

- A Low pass filter with two resistors and one capacitor output is connected to threshold and trigger terminals
- Discharge terminal is connected in between the two resistors

OPERATION:

- Initially, output of the 555 timer is HIGH. So transistor Q2 is ON. Capacitor voltage is zero. So, now it tries to charge up to max. value Vcc with time constant.

$$\tau = (R_A + R_B)C$$



At $t = t_1$, V_c crosses $\frac{1}{3}V_{CC}$

- At $t = t_1^+$, $V_c > \frac{1}{3}V_{CC}$ and $V_c < \frac{2}{3}V_{CC}$

So. Thres $< \frac{2}{3}V_{CC}$ · R = 0

Trig $> \frac{1}{3}V_{CC}$ S = 1

Output = 1 [HIGH]

So, output $\bar{Q}$ = LOW, so Q_2 is OFF so capacitor charges.

- At $t = t_2$, capacitor value crosses $\frac{2}{3}V_{cc}$

So, $t = t_2^+$ $V_c > \frac{2}{3}V_{cc}$ $V_c > \frac{1}{3}V_{cc}$

Thresh $> \frac{2}{3}V_{cc}$ R=1

Trig $> \frac{1}{3}V_{cc}$ S=0

Output = 0 [LOW]

So, $\bar{Q}$ is high. So Q_2 transistor is ON. So. capacitor is connected to ground through resistor R_B. It tries to discharge upto 0V. with time constant $\tau = RC$

- But at $t = t_3$ it tries to cross $\frac{1}{3}V_{cc}$

$V_c < \frac{1}{3}V_{cc}$ and $V_c < \frac{2}{3}V_{cc}$

Thresh $< \frac{2}{3}V_{cc}$ R=0

Trig $< \frac{1}{3}V_{cc}$ PS=1

Output = 1 [HIGH]

So, $\bar{Q}$ = LOW so Q_2 is OFF so capacitor tries to charge upto V_{cc}.

- So, V_c value will not exceed $\frac{2}{3}V_{cc}$ and will not decrease than $\frac{1}{3}V_{cc}$. when capacitor is charging output is high, when capacitor is discharging output is low

- capacitor is charging with time constant $(R_A + R_B)C$
- capacitor is discharging with time constant R_BC

CALCULATION OF T_{ON}:

$= t_2 - t_1 = t_4 - t_3 = t_6 - t_5 = \ldots$

While this duration, capacitor is trying to charge upto V_{cc} from $\frac{1}{3}V_{cc}$ with time constant $(R_A + R_B)C$

So,

$$V_i = \frac{1}{3}V_{cc}, \quad V_f = V_{cc} \quad \tau = (R_A + R_B)C$$

$$V_c(t) = V_{cc} + \left(\frac{1}{3}V_{cc} - V_{cc}\right) e^{-t/(R_A+R_B)C}$$

at $t = T_{ON}$

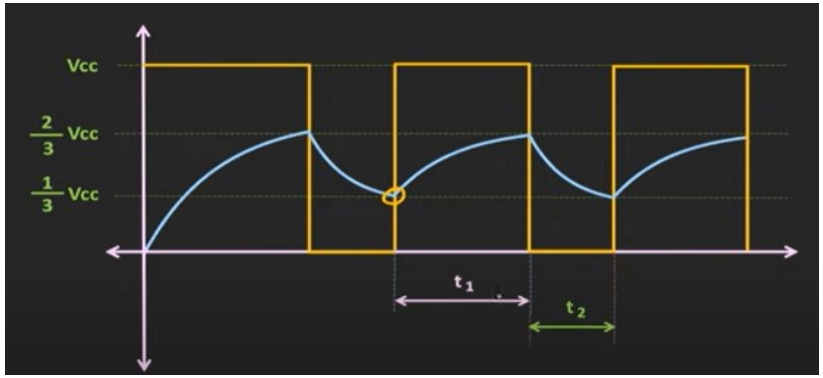
$$= V_c(T_{ON}) = \frac{2}{3}V_{cc}$$

$$\frac{2}{3}V_{cc} = V_{cc}\left[1 - \frac{2}{3}e^{-T_{ON}/(R_A+R_B)C}\right]$$

$$\frac{2}{3}e^{-T_{ON}/(R_A+R_B)C} = \frac{1}{3}$$

$$T_{ON} = (R_A + R_B)C \ln 2$$

$$\boxed{T_{ON} = 0.69(R_A + R_B)C}$$



CALCULATION OF T_{OFF}

$t_3 - t_2 = t_5 - t_4 = t_7 - t_6 = \ldots$

While this duration capacitor is discharging from $\frac{2}{3} V_{CC}$ to zero with time constant $R_B.C$

So, $V_i = \frac{2}{3} V_{CC}$, $V_f = 0$ $\quad \tau = R_B C$

So,

$$V_c(t) = 0 + \left(\frac{2}{3} V_{CC} - 0 \right) e^{-t/R_B C} .$$

At $t = T_{OFF}$

$$V_c(T_{OFF}) = \frac{1}{3} V_{CC}$$

$$\frac{1}{3} V_{CC} = \frac{2}{3} V_{CC} \cdot \bar{e}^{\,T_{OFF}/R_B C}$$

$$T_{OFF} = R_B C \ln 2$$

$$\boxed{T_{OFF} = 0.69\, R_B C}$$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100$$

$$= \frac{0.69 (R_A + R_B) C}{0.69 (R_A + 2R_B) C} \times 100$$

$$\% D = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

$R_1 > R_2 \Rightarrow D > 50\%$.

$R_1 < R_2 \Rightarrow D < 50\%$.

Applications of astable multivibrator:

1. FSK generator
2. Pulse Position Modulator

FSK Generator:

FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal. The circuit is as shown in Fig. 8.21. The standard digital data input frequency is 150 Hz. When input is HIGH, transistor Q is ***off*** and 555 timer works in the normal astable mode of operation. The frequency of the output waveform given by Eq. (8.1) can be rewritten as

$$f_o = \frac{1.45}{(R_A + 2R_B)C} \tag{8.18}$$

In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals. The components R_A and R_B and the capacitor C can be selected so that f_o is 1070 Hz.

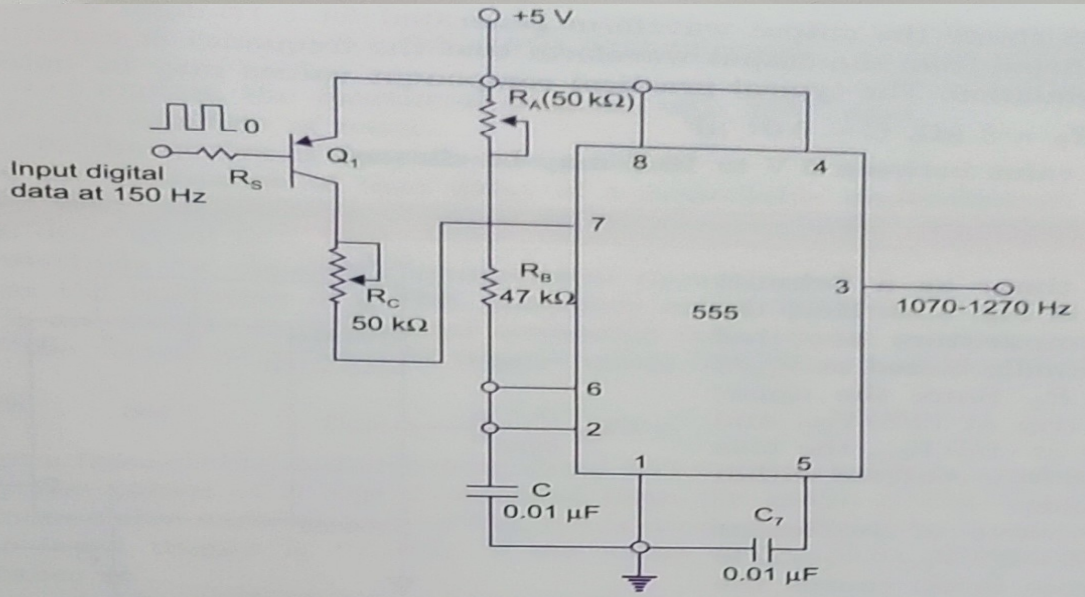


Fig. 8.21 FSK generator

When the input is LOW, Q goes ***on*** and connects the resistance R_C across R_A. The output frequency is now given by

$$\frac{1.45}{(R_A \parallel R_C) + 2R_B} \tag{8.19}$$

The resistance R_C can be adjusted to get an output frequency 1270 Hz.

Pulse-Position Modulator

The pulse-position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation as shown in Fig. 8.22. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is

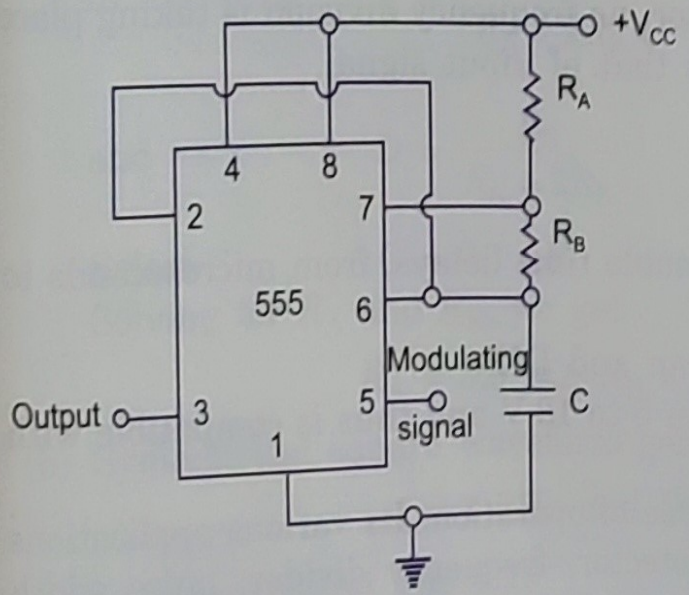


Fig. 8.22 Pulse position modulator

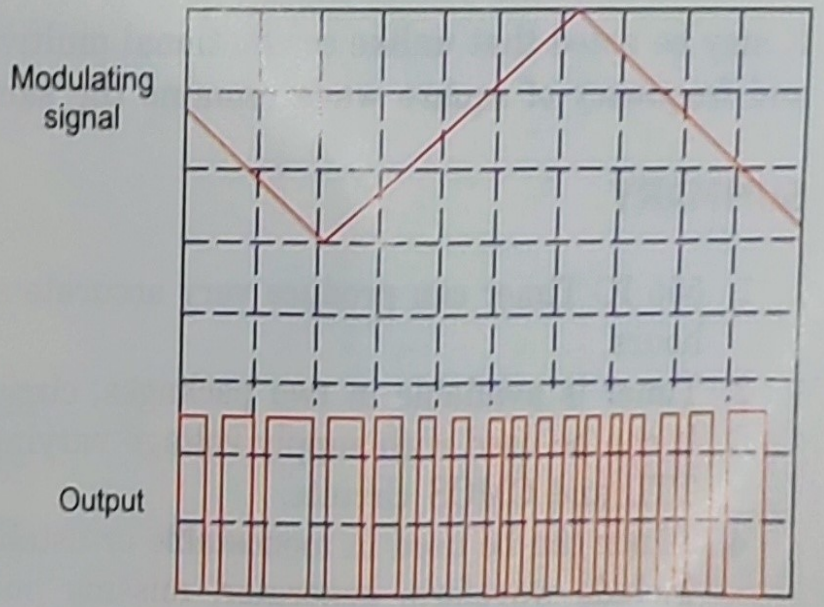


Fig. 8.23 Pulse position modulator output

1. Design Astable multivibrator at 1Khz frequency and its duty cycle is 50%.

Solution: if duty cycle is 50, R1 = R2 = R. T= T_{ON} +T_{Off}

T_{ON} = 0.693 R_1 C T_{Off} = 0.693 R_2 C

For 50% duty cycle, R1=R2, T = 0.693(2R1) X C

F = 1Khz, T= 1/f = 1ms

For astable multivibrator, Total time period T =0.693 (R1+R2)C

Assume C = 0.1microfarads

1x 10^{-3}=0.693(2R1)x0.1x10^{-6}

R1= 720 ohms

2. Design Astable multivibrator using 555 timer of output frequency of 5Khz and its duty cycle is 70%.

Solution: if duty cycle is greater than 50 i.e D>50

T_{ON} = 0.693 (R_A+R_B) C and Toff = 0.693 R_B C

Given f = 1 Khz D= 50%

T= 1/f = 200micro seconds

D= (T_{ON} / T) *100

TON = D X T = 70% X 200μs = 140 μs

D>50 assume C= 0.1 μf

T_{ON} = 0.693 (R_A+R_B) C

Submit R_B = 600 Ω in above

RA = 1420.20 Ω

Solution: if duty cycle is less than 50 i.e D<50

T_{ON} = 0.693 R_AC and Toff = 0.693 R_B C

T = TON + Toff

T_{off} = T-T_{ON} = 200 – 140 = 60 μs

Toff = 0.693 R_B C asumeC= 0.1 μf

60 = 0.693 R_B X 0.1X 10^{-6}

R_B = 600Ω

Voltage-controlled oscillator (VCO):IC566

A voltage-controlled oscillator (VCO) is **an electronic oscillator whose oscillation frequency is controlled by a voltage input**.

Frequency Control in Voltage Controlled Oscillator

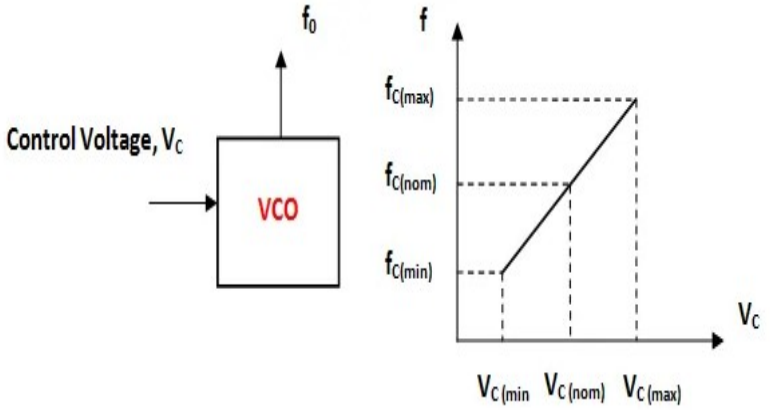
Many forms of VCOs are generally used. It can be of RC oscillator or multi vibrator type or LC or crystal oscillator type. However; if it is of RC oscillator type, the oscillation frequency of output signal will be in inversely proportional to capacitance as $f = \frac{1}{(2\pi RC)}$

In the case of LC oscillator, the oscillation frequency of output signal will be

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

So, we can say that as the input voltage or control voltage increases, the capacitance get reduced. Hence, the control voltage and frequency of oscillations are directly proportional. That is, when one increases, the other will increase. **C= Q / V**

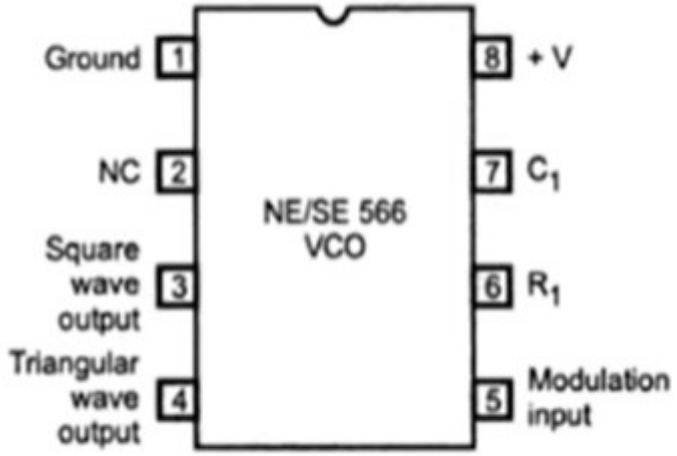
we can see that at nominal control voltage represented by $V_{C(nom)}$, the oscillator works at its free running or normal frequency, $f_{C(nom)}$. As the control voltage decreases from nominal voltage, the frequency also decreases and as the nominal control voltage increases, the frequency also gets higher



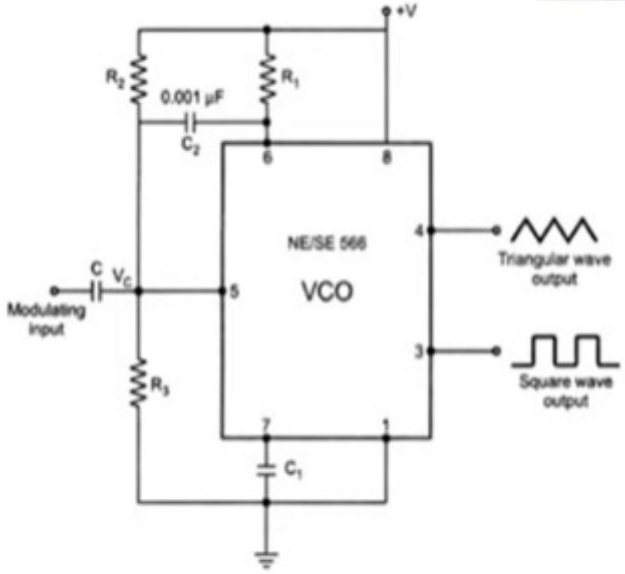
Voltage Controlled Oscillator (IC 566)

The VCO generates an output signal frequency that is directly proportional to its input voltage. Typical example of VCO is Signetics NE/SE 566 VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage. The block diagram of the VCO is shown in Fig 2.12. The frequency of oscillations is determined by three external R1 and capacitor C1 and the voltage VC applied to the control terminal 5. This type of circuit is also called a voltage-to-frequency converter (VFC).

The triangular wave is generated by alternatively charging the external capacitor C1 by one current source and then linearly discharging it by another. The charging and discharging levels are determined by Schmitt trigger action. The schmitt trigger also provides square wave output. Both the wave forms are buffered so the output impedance of each is 50 ohms.

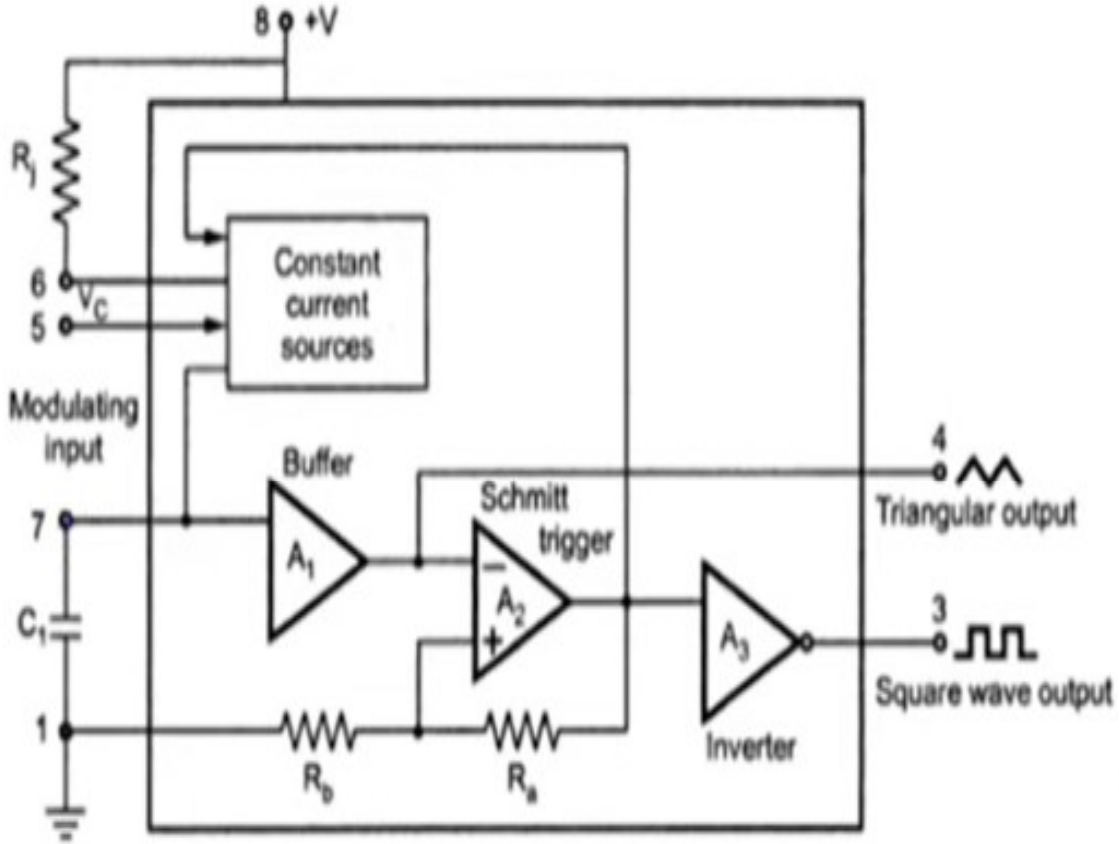


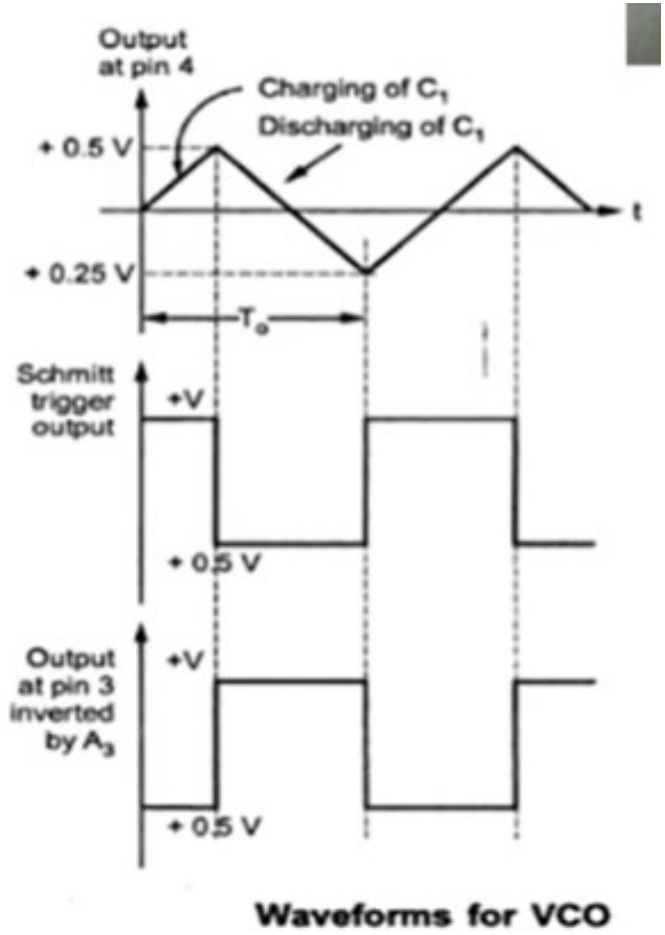
Pin diagram of IC 566 VCO



Typical connection diagram of 566 VCO

In this arrangement the R1C1 combination determines the free running frequency and the control voltage VC at pin 5 is set by voltage divider formed with R2 and R3.





Waveforms for VCO

$$f_o = \frac{2(+V - V_C)}{C_1 R_1 (+V)}$$

The modulating voltage also called a control voltage is applied to the modulating input (pin 5). The external capacitor charges or discharges from the constant current source. The charging current is controlled by the modulating signal or the by the external resistor R1.

The charging voltage is decided by the Schmitt trigger. The Schmitt trigger output swings between Vcc and 0.5 Vcc. The voltage across the capacitor is applied to the buffer amplifier. If Ra = Rb, the input to the non inverting input of the Schmitt Trigger changes from 0.5 Vcc to 0.25 Vcc. When the capacitor voltage goes beyond 0.5 Vcc, the output of the Schmitt Trigger becomes low (0.5Vcc). Now the capacitor discharges. When the capacitor voltage goes below 0.25 Vcc, the output of the Schmitt trigger becomes high (Vcc). Because of the constant current source, the capacitor take equal timings for charging and discharging. Hence the output will be a perfect triangular one. This is available at Pin 4. The output of the Schmitt trigger is a step voltage. So the output at Pin 3 will be a square wave.

$$\text{The output frequency is given by } fo = \frac{2\,(Vcc - Vc)}{CtRt\,(Vcc)}$$

The figure shows that the LM566 IC contains current sources to charge and discharge an external capacitor at a rate set by an external resistor R1 and the modulating dc input voltage V.

For a Voltage controlled oscillator generating a sawtooth waveform, the main component is the capacitor who's charging and discharging decides the formation of the output waveform. The input is given in form a voltage that can be controlled. This voltage is converted to a current signal and is applied to the capacitor. As the current passes through the capacitor, it starts charging and a voltage starts building across it. As the capacitor charges and the voltage across it increase gradually, the voltage is compared with a reference voltage using a comparator.

When the capacitor voltage exceeds the reference voltage, the comparator generates a high logic output that triggers the transistor, and the capacitor is connected to the ground and starts discharging. Thus the output waveform generated is the representation of the charging and discharging of the capacitor and the frequency is controlled by the input dc voltage.

VOLTAGE TO FREQUENCY CONVERTER:

- V-F conversion factor is a very important parameter for VCO

$$K_v = \frac{\Delta f_o}{\Delta V_c}$$

ΔV_c = change in the control voltage producing change of Δf_o in the frequency.

Let f'_o = New frequency

f_o = original frequency

$$\Delta f_o = f'_o - f_o \text{ w}$$

- While V_c is changed by ΔV_c to achieve this,
- From expression of f'_o ,

$$f'_o = \frac{2[+V-(V_c-\Delta V_c)]}{C_1 R_1 (+V)} \qquad f_o = \frac{2[+V-(V_c)]}{C_1 R_1 (+V)}$$

$$\Delta f_o = f_2 - f_1 = \frac{2\Delta V_c}{C_1 R_1 (+V)}$$

$$\Delta V_c = \frac{R_1 C_1 \Delta f_o (+V)}{2} \quad \rightarrow (1)$$

- With no modulating input voltage,
- Control voltage V_c = (7/8)(+V)
- If fo is the original frequency then, $f_o = \frac{2\left[+V - \frac{7}{8}(V)\right]}{C_1 R_1 (+V)} = \frac{0.25}{C_1 R_1}$

using the value of R1 C1 from the (1) $f_o = \frac{0.25}{\frac{2\Delta V_c}{f_o (+V)}}$

$$K_v = \frac{\Delta f_o}{\Delta V_c} = \frac{f_o}{0.125(+V)}$$

$$\boxed{K_v = \frac{8 f_o}{(+V)}}$$

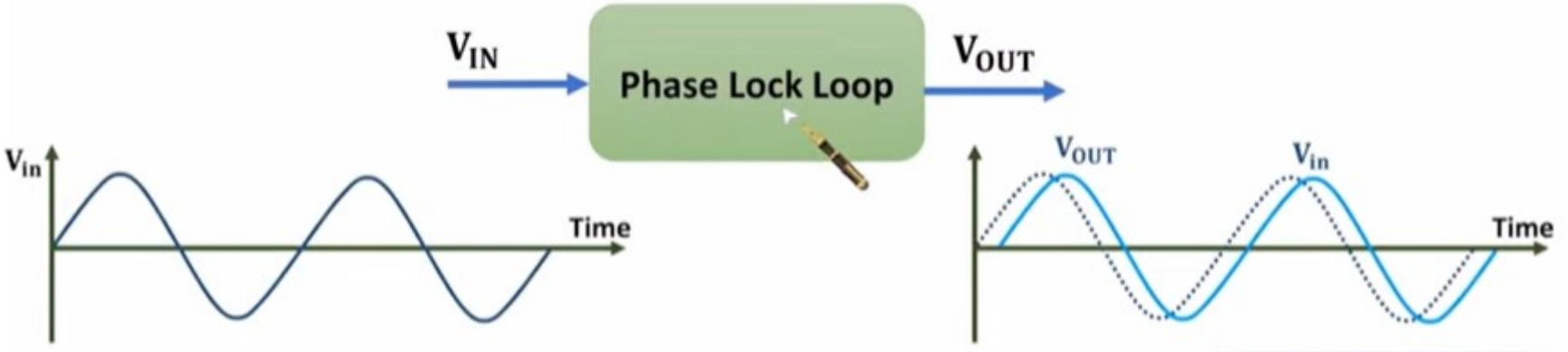
- Where fo is the original frequency
- This is the required voltage to frequency conversion factor.

Applications

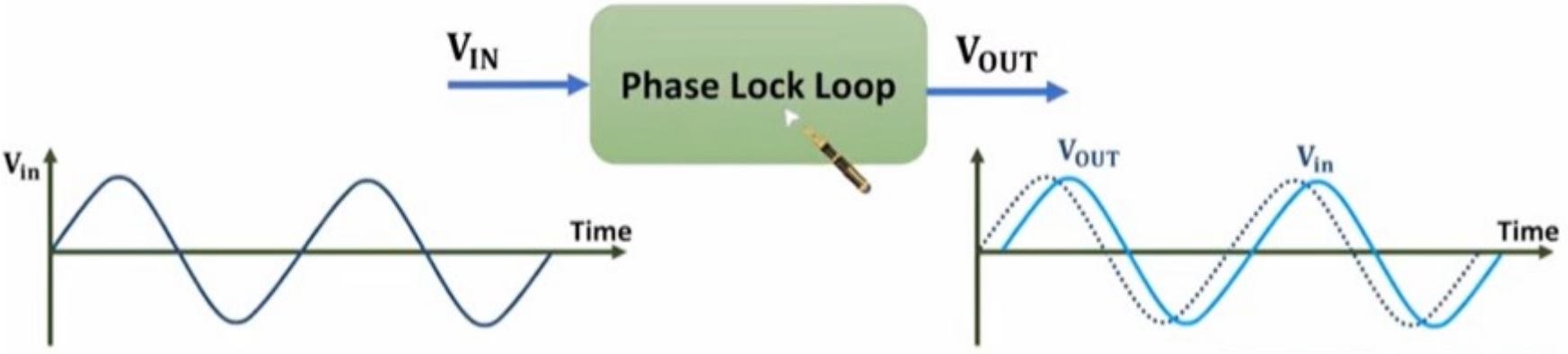
Phase Lock Loop

Modulation and Demodulation Circuits

- It is used for timing synchronization of signals.
- It is used to lock the phase and frequency of the input signal.



- It is used for timing synchronization of signals.
- It is used to lock the phase and frequency of the input signal.



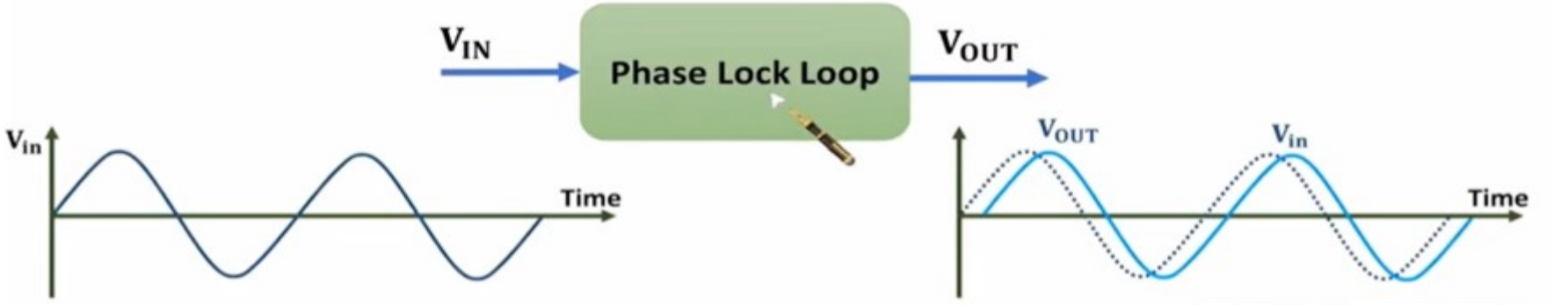
Phase Locked Loop (PLL): It is one of the vital blocks in linear systems. It is useful in communication systems such as radars, satellites, FMs, etc.
In present, the PLL is now readily available as IC‟s which were developed in the SE/NE 560 series. Some of the commonly used ones are the SE/NE 560, 561, 562, 564, 565 and 567.The difference between each one of them is in the different parameters like operating frequency range, power supply requirements, and frequency and bandwidth ranges. Out of all the series, the SE/NE 565 is the most famous. It is available as a 14-pin DIP and also as a 10-pin metal can package.

A **phase-locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal.**

It **synchronize** the input and output signals in **Frequency as well as Phase.**

If Output frequency f_{OUT} = Input frequency f_{IN}
And phase difference between input and output $\Delta\Phi = 0$ or consta
Then PLL, lock the signal at output side.

- It is used for timing synchronization of signals.
- It is used to lock the phase and frequency of the input signal.

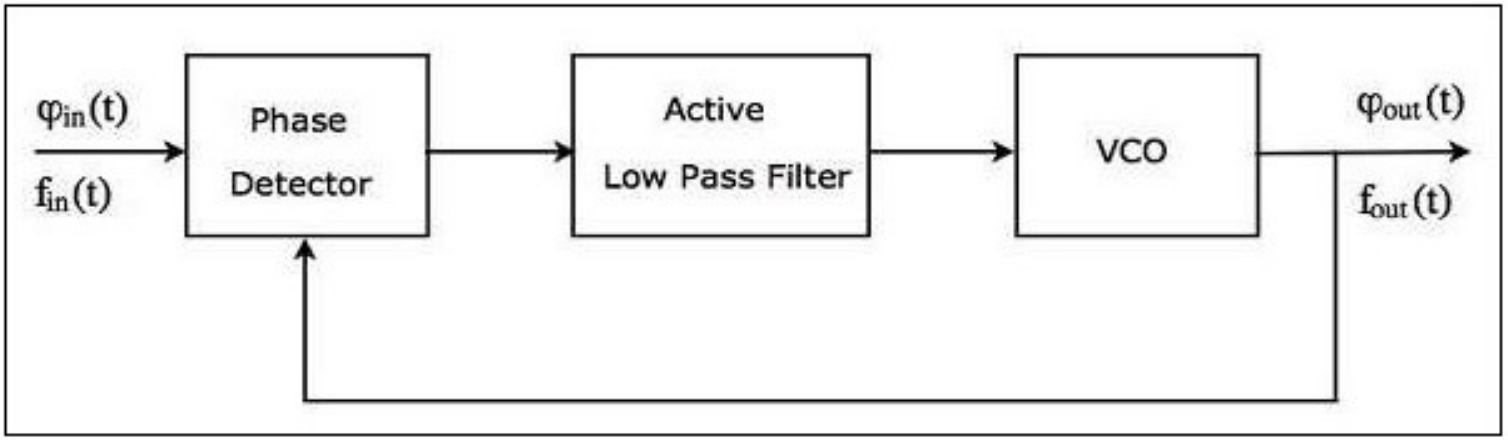


Block Diagram of PLL

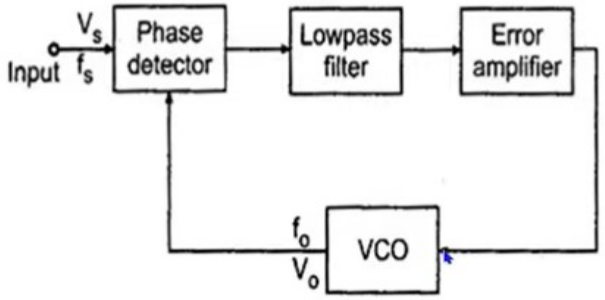
A Phase Locked Loop (PLL) mainly consists of the following **three blocks** −

- Phase Detector
- Active Low Pass Filter
- Voltage Controlled Oscillator (VCO)

The **block diagram** of PLL is shown in the following figure −



The output of a phase detector is applied as an input of active low pass filter. Similarly, the output of active low pass filter is applied as an input of VCO



The **working** of a PLL is as follows −

- **Phase detector** produces a DC voltage, which is proportional to the phase difference between the input signal having frequency of f_{in} and feedback (output) signal having frequency of f_{out} .
- A **Phase detector** is a multiplier and it produces two frequency components at its output − sum of the frequencies f_{in} and f_{out} and difference of frequencies f_{in} & f_{out} .
- An **active low pass filter** produces a DC voltage at its output, after eliminating high frequency component present in the output of the phase detector. It also amplifies the signal.
- A **VCO** produces a signal having a certain frequency, when there is no input applied to it. This frequency can be shifted to either side by applying a DC voltage to it. Therefore, the frequency deviation is directly proportional to the DC voltage present at the output of a low pass filter.

The above operations take place until the VCO frequency equals to the input signal frequency. Based on the type of application, we can use either the output of active low pass filter or output of a VCO. PLLs are used in many **applications** such as FM demodulator, clock generator etc.

VCO (Voltage Controlled Oscillator): Runs in free running mode with output frequency of f_o. The non-zero control voltage results in a shift in the VCO frequency from its free running frequency f_o to a frequency f, given by

$$f = f_o + k_v V_c$$

- Where, K_v = voltage to frequency transfer coefficient of VCO

The above operations take place until the VCO frequency equals to the input signal frequency. Based on the type of application, we can use either the output of active low pass filter or output of a VCO. PLLs are used in many **applications** such as FM demodulator, clock generator etc.

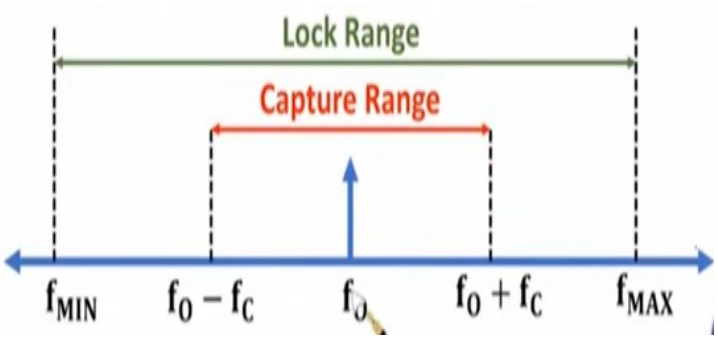
PLL operates in one of the **following three modes** −

- Free running mode
- Capture mode
- Lock mode

Initially, PLL operates in **free running mode** when no input is applied to it. When an input signal having some frequency is applied to PLL, then the output signal frequency of VCO will start change. At this stage, the PLL is said to be operating in the **capture mode**. The output signal frequency of VCO will change continuously until it is equal to the input signal frequency.

- **Lock Range:**
- When the PLL is n lock, it can track frequency changes in the incoming signal is called the Lock Range or tracking range of the PLL.
- It is expressed in percentage of f_o, the VCO frequency.

Capture range: The range of input frequencies that the PLL can capture to lock onto an input signal. This is the range of frequencies that the voltage controlled oscillator (VCO) can produce.



Lock range: The range of frequencies that the PLL can track and adjust to once it has locked onto an input signal. The lock range is wider than the capture range.

Pull in time: The total time taken by the loop to obtain lock is called pull in time. It depends on the initial phase and frequency difference between the two input signals, the overall loop gain and the loop filter characteristics.

Capture Range

The range of input frequencies around the VCO center frequency onto which the loop can lock when starting from the unlocked condition.

Lock Range

The range of input frequencies over which the loop remain in the lock condition once it has captured the input signal.

Phase Detector / Phase Comparator:

The comparator circuit compares the input frequency and the VCO output frequency and produces a dc voltage that is proportional to the phase difference between the two frequencies.
In other words, a phase detector or phase comparator is basically a frequency mixer (or) analog multiplier (or) logic circuit that generates a voltage signal which represents the difference in phase between two signal inputs.

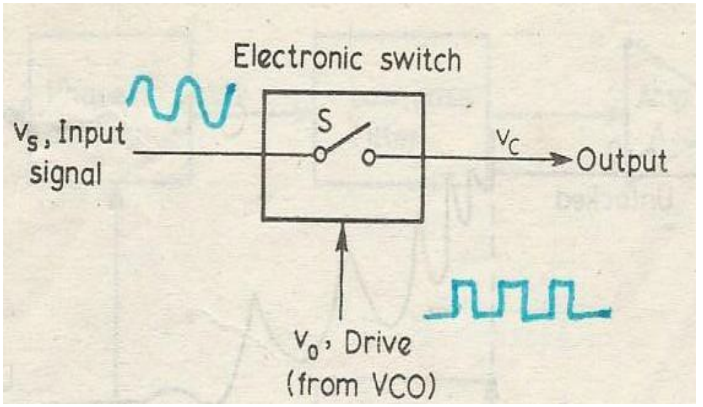
Types of Phase Detector

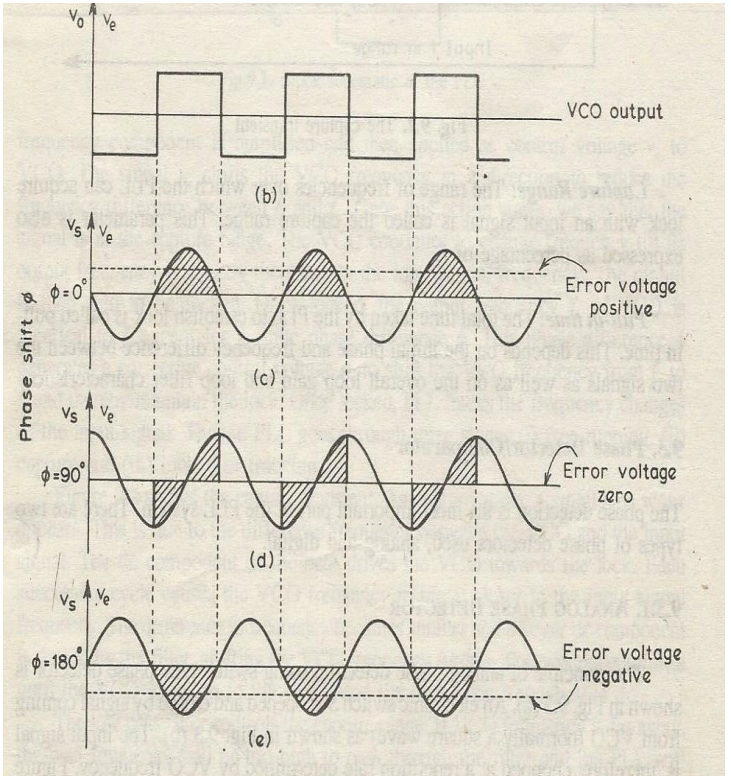
1. Analog type
    a. Electronic switch
    b. Doubled balanced mixer circuit (Balanced Modulator)
2. Digital type
    a. Using XOR
    b. Using S-R flip flop

Electronic Switch type Phase Detector:

This is basically an electronic switch.. The switch is opened or closed by a square signal from VCO. Thus the input analog signal is chopped by the frequency determined by the VCO frequency. The switch is closed when the VCO output is positive and opens when the VCO output is negative.

1. When Vs and Vo are in phase (ø = 0): As the switch S is closed only for the positive output of VCO, the error voltage Ve is only the half positive portions of the input is permitted to cross the switch. Thus the average output i.e error voltage Ve is positive.
2. When Vs and Vo are out of phase by 90 (ø = 90): The switch closed for half of the Negative and the other half of the positive input. Thus the average output is zero. The error voltage Ve is zero.
3. When Vs and Vo are out of phase by 180 (ø = 180): The switch closed for negative half cycles of the input and opens for the positive half cycle of the input. Thus the average output is negative. The error voltage Ve is negative.





From the fig it is clear that

1. the error voltage is zero, when the phase shift between the two input is 90˚
2. the error voltage is positive, when the phase shift between the two input is < 90˚
3. the error voltage is negative, when the phase shift between the two input is > 90˚

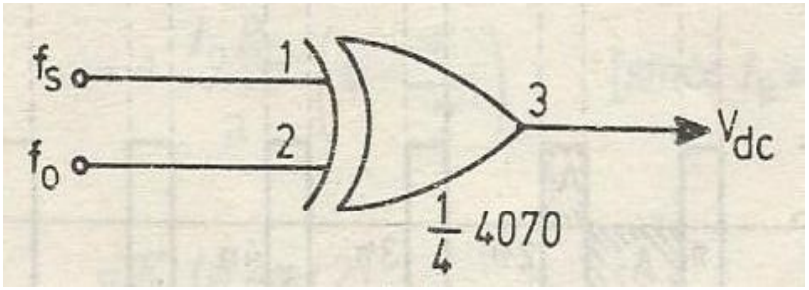
In this type of Phase comparator, the phase information for only one half of the input waveform is detected and averaged. So, it is called as half wave detector. The output of the phase comparator is filtered and the error signal is obtained.

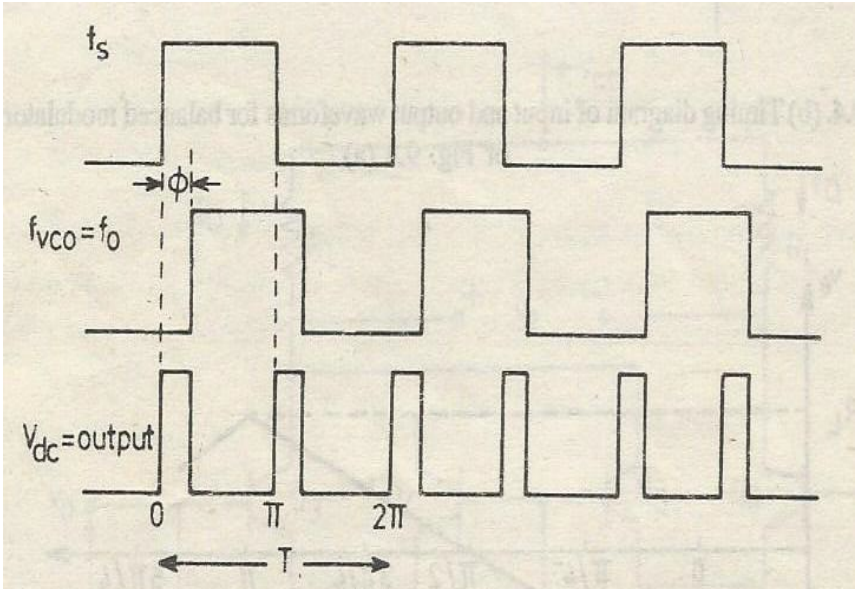
Drawbacks: The output is proportional to cos ø and not proportional to ø, making it non linear.

Digital Phase Detector:

It is obtained as a CMOS IC of type 4070. Both the frequencies fs and fo are provided as an input to the EX OR phase detector. In EX-OR concept the output becomes HIGH only if either of the inputs fs or fo becomes HIGH. All other conditions will produce a LOW output.

The figure shows the graph DC output voltage as a function of the phase difference between fs and fo. The output DC voltage is maximum when the phase detector is 180°.This type of phase detector is used when both fs and fo are square waves.





PLL Applications

- Demodulation of both FM and AM signals
- Stereo Decoders.
- Frequency synthesis that provides multiple of a reference signal frequency.
- Used in motor speed controls, tracking filters.
- Used in frequency shift keying (FSK) decodes for demodulation carrier frequencies.
- Recovery of small signals that otherwise would be lost in noise
- Recovery of clock timing information from a data stream such as from a disk drive
- Clock multipliers in microprocessors
- DTMF decoders, modems, and other tone decoders, for remote control and telecommunications
- DSP of video signals
- Atomic force microscopy

Monolithic phase locked loop (IC 565):

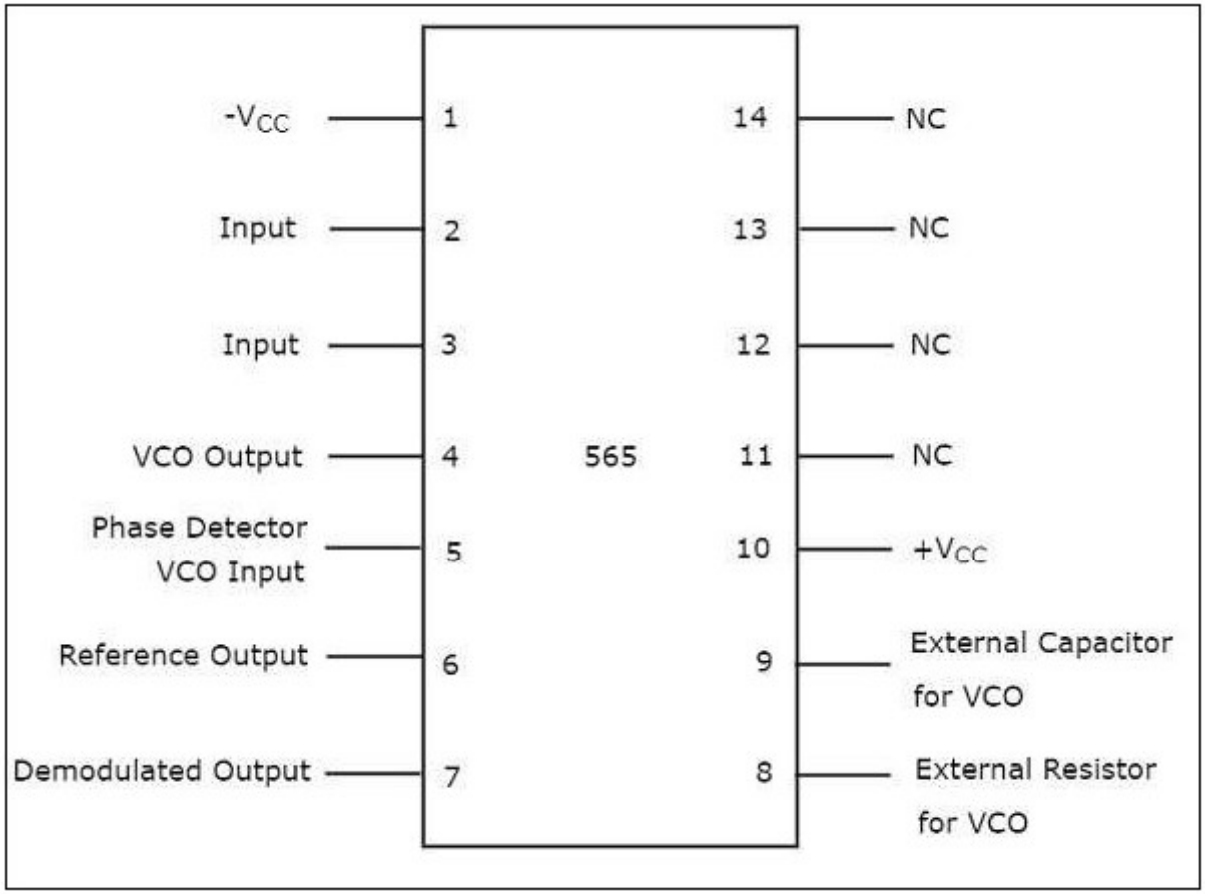
All the different blocks of PLL are available in a single chip of IC 565.

- 14 pin DIP package or 10 pin metal can package.

$$f_o = \frac{1.2}{4 R_T C_T} \text{ Hz}$$

- R_T, C_T = external resistor & capacitor
- R_T = between 2KΩ to 20 K Ω
- f_o adjusted with R_T, C_T

IC 565


-Vcc
1
Input
2
Input
3
VCO Output
4
Phase Detector
VCO Input
5
Reference Output
6
Demodulated Output
7
565
14
NC
13
NC
12
NC
11
NC
10
+Vcc
9
External Capacitor
for VCO
8
External Resistor
for VCO

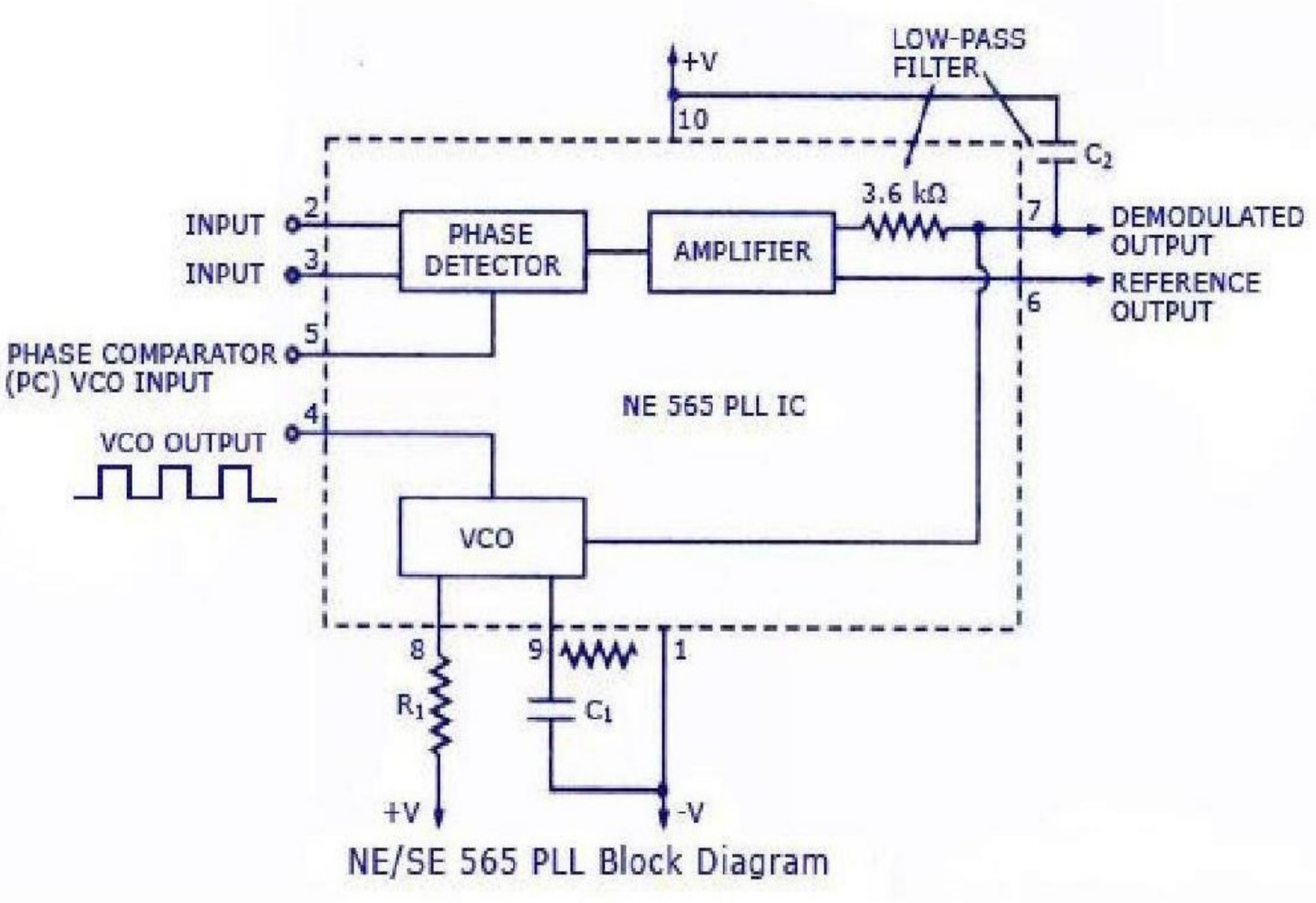


Fig 2.14 Block Diagram of IC 565

Fig shows the pin diagram and block diagram of IC 565 PLL. It consists of phase detector, amplifier, low pass filter and VCO.As shown in the block diagram the phase locked feedback loop is not internally connected. Therefore, it is necessary to connect output of VCO to the phase comparator input, externally.

In frequency multiplication applications a digital frequency divider is inserted into the loop i.e., between pin 4 and pin 5. The centre frequency of the PLL is determined by the free-running frequency of the VCO and it is given by

$$f_o = \frac{1.2}{4R_1C_1}$$

Where R1 and C1 are an external resistor and capacitor connected to pins 8 and 9, respectively. The values of R1 and C1 are adjusted such that the free running frequency will be at the centre of the input frequency range. The values of R1 are restricted from 2 kΩ to 20 kΩ,but a capacitor can have any value. A capacitor C2 connected between pin 7 and the positive supply forms a first order low pass filter with an internal resistance of 3.6 kΩ. The value of filter capacitor C2 should be larger enough to eliminate possible demodulated output voltage at pin 7 in order to stabilize the VCO frequency

The PLL can lock to and track an input signal over typically ±60% bandwidth w.r.t fo as the center frequency. The lock range fL and the capture range fC of the PLL are given by the following equations.

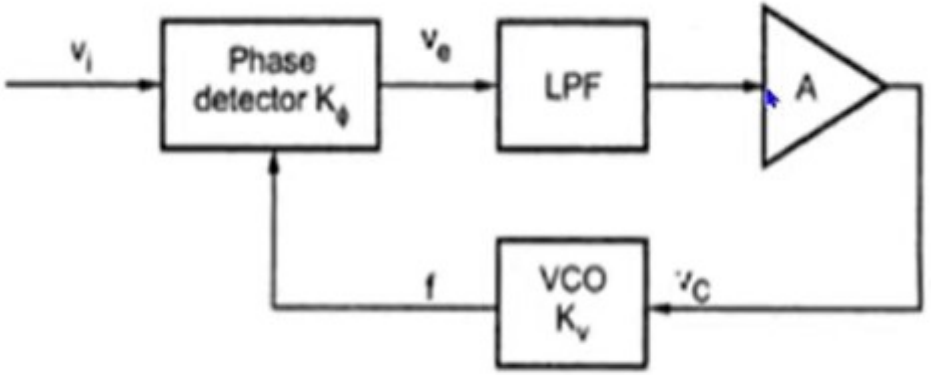
$$f_L = \pm \frac{8 f_0}{V}$$

Where fo=free running frequency And V=(+V)-(-V)Volts And

$$f_C = \pm \sqrt{\frac{f_L}{2\pi(3.6)10^3 C_2}}$$

From above equation the lock range increases with an increase in input voltage but decrease with increase in supply voltage. The two inputs to the phase detector allows direct coupling of an input signal, provided that there is no dc voltage difference between the pins and the dc resistances seen from pins 2 and 3 are equal.

Derivation of lock range:



PLL block diagram to determine lock-range

- Output voltage of a phase detector is
- $V_e = k_\phi(\phi - \prod/2) \rightarrow (1)$
- Where, ϕ = phase error
- The output voltage of a phase detector is filtered by the low pass filter to remove the high frequency component.

K is phase coefficient

- The output of the filter is amplified by a gain A and then applied as the control voltage V_c to the Vco as given by
- $V_c = A V_e = A k_\phi(\phi - \Pi/2) \rightarrow (2)$
- This control voltage V_c will result in a shift in the Vco frequency from its center frequency f_o to a frequency f,
- $f = f_o + k_v V_c \rightarrow (3)$
- When the PLL is locked, the input frequency is given by $f = f_i = f_o + K_v v_C$
- Sub Vc value from eq(2)

$$f_i - f_o = K_v K_\phi A(\theta_e - \pi/2)$$

$$\theta_e - \frac{\pi}{2} = \frac{f_i - f_o}{K_v K_\phi A}$$

$$\theta_e = \frac{\pi}{2} + \frac{f_i - f_C}{K_v K_\phi A}$$

- The Vo(max) available from the phase detector occurs for $\phi = \prod$ and 0

$$v_e(max) = \pm K_\phi(\pi/2)$$

- Corresponding maximum control voltage is

$$v_C(max) = \pm K_\phi(\pi/2)A$$

- Sub Vc value in f equation,

$$f = f_i = f_o \pm K_v K_\phi(\pi/2)A$$
$$= f_o \pm \Delta f_L$$

- Where 2 ΔfL will be lock-in frequency range given by $\text{lock range} = 2\Delta f_L = K_v K_\phi A\,\pi \therefore \Delta f_L = K_v K_\phi A\,\pi/2$

$$K_v = \frac{8 f_o}{V}$$

Where $V = V_{cc} - (-V_{cc})$

For PLL 565, $K_\phi = \frac{1.4}{\pi}$ and A = 1.4

Substituting these values we get,

$$\Delta f_L = \pm \frac{8 f_o}{V} \times \frac{1.4}{\pi} \times 1.4 \times \frac{\pi}{2}$$

$$\Delta f_L = \pm \frac{7.84 f_o}{V}$$

Lock in range is

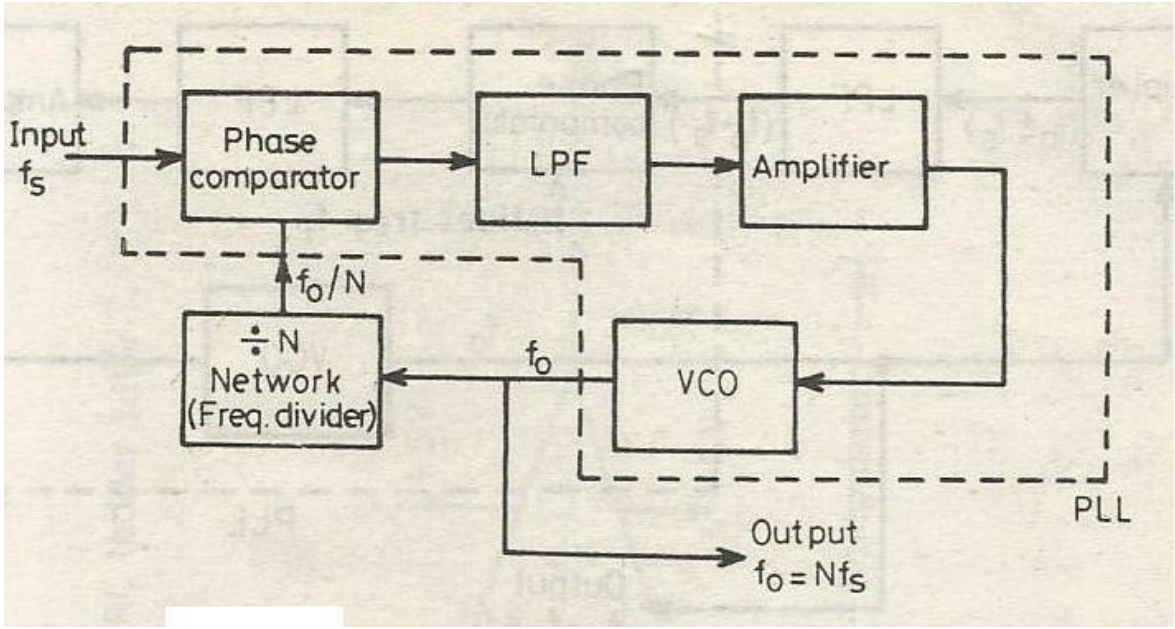
$$\Delta f_L = \pm \frac{7.84 f_o}{V}$$

- The equation for capture range of PLL is given by

$$\Delta f_{cap} = \pm \left[\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C} \right]^{1/2}$$

Applications of PLL:

Frequency multiplier:



This circuit contains a Phase Comparator , Low Pass Filter, Error Amplifier and Voltage controlled Oscillator and a divide by N counter. The input frequency fs is applied to the phase comparator. The another input to the phase comparator is the output of the counter.

The phase comparator compares the two input frequencies and delivers an error signal, This signal is amplified and fed to the Voltage controlled Oscillator.

The output frequency of the VCO depends on the amplitude of the error signal. By adjusting the VCO, the PLL is made to lock. Under locked condition the two input frequencies of the Phase Comparator are equal

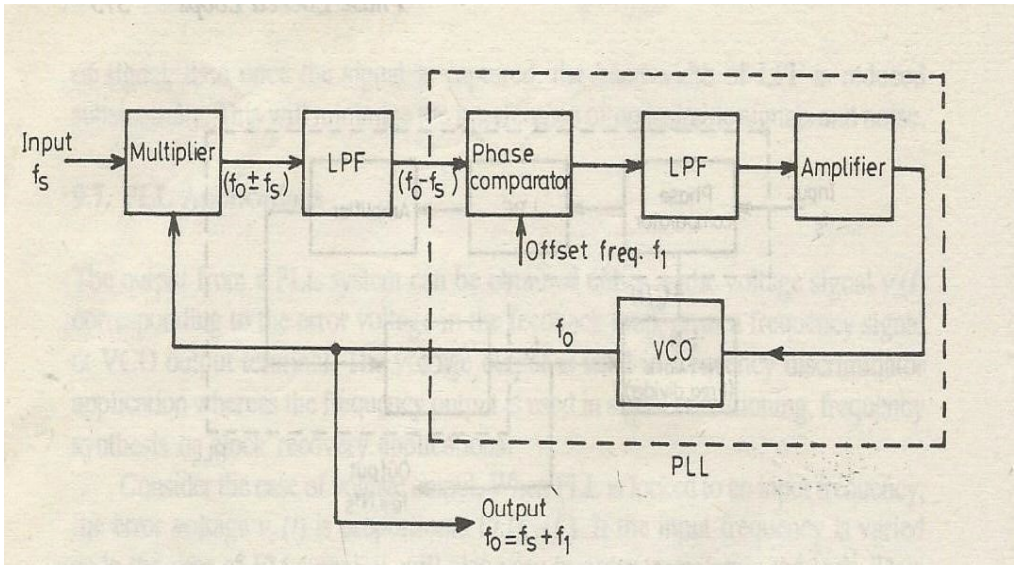
i.e. fs = fo / N

Thus, fo = N X fs.

The input frequency is multiplied by a scalar N. By properly selecting N, any high frequency can be developed.

Frequency translation: Frequency translation is nothing but shifting the given frequency to a nearby level either in the positive or negative direction

The input frequency fs is to be shifted by an offset frequency fi . The input frequency fs is fed to the mixer. The other input to the mixer is the frequency fo from the voltage controlled oscillator. The mixer mixes the two signals and produce a sum and difference frequencies (fo+fs) and (fo-fs)



These frequencies are applied to a low pass filter. This LPf allows only the low frequency (fo-fs) and filters out the high frequency (f0+fs) The output frequency (fo – fs) of LPF is fed to a phase comparator. The offset frequency fi (fi ‹‹ fs) is fed to the other input of the phase comparator. The phase comparator compares the two inputs and delivers an error signal. This error signal is amplified and applied as an input to the VCO. The amplitude of this error signal decides the output frequency of the VCO. Now the VCO is made to track the input frequency. At one point the loop is locked, Under locked condition, the two input frequencies of Phase Comparator are equal. fo – fs = fi ,

Rearranging, fo = (fs + fi) i.e. the input frequency fs is shifted / translated to a new value fs + fi.

9.7.3 AM Detection

A PLL may be used to demodulate AM signals as shown in Fig. 9.14. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

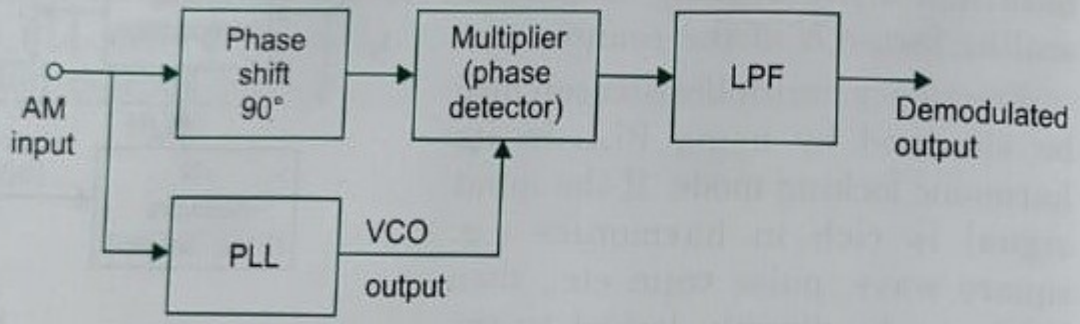
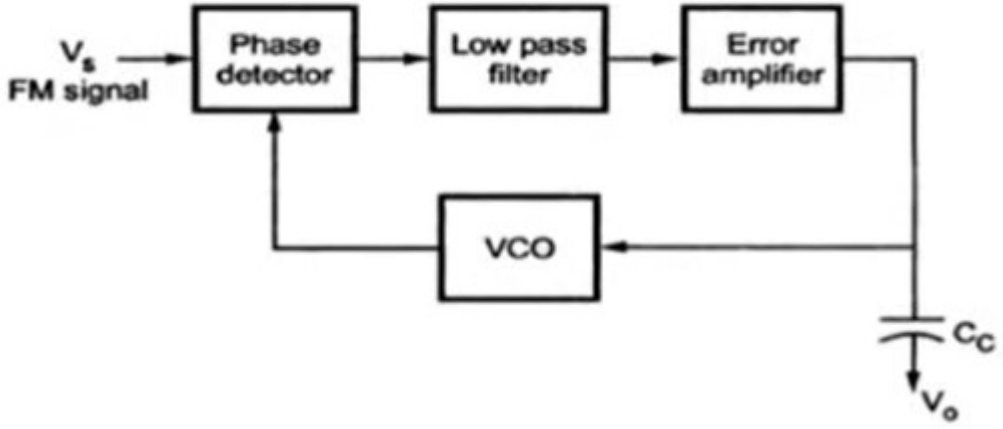


Fig. 9.14 PLL used as AM demodulator

- FM Demodulator:



If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

9.7.3 AM Detection

A PLL may be used to demodulate AM signals as shown in Fig. 9.14. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

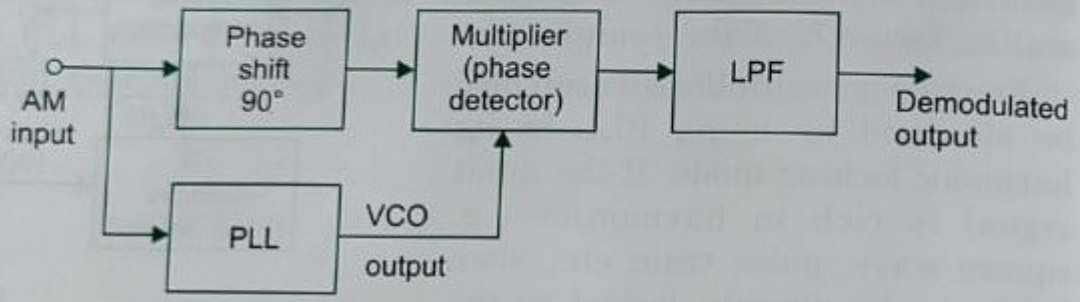
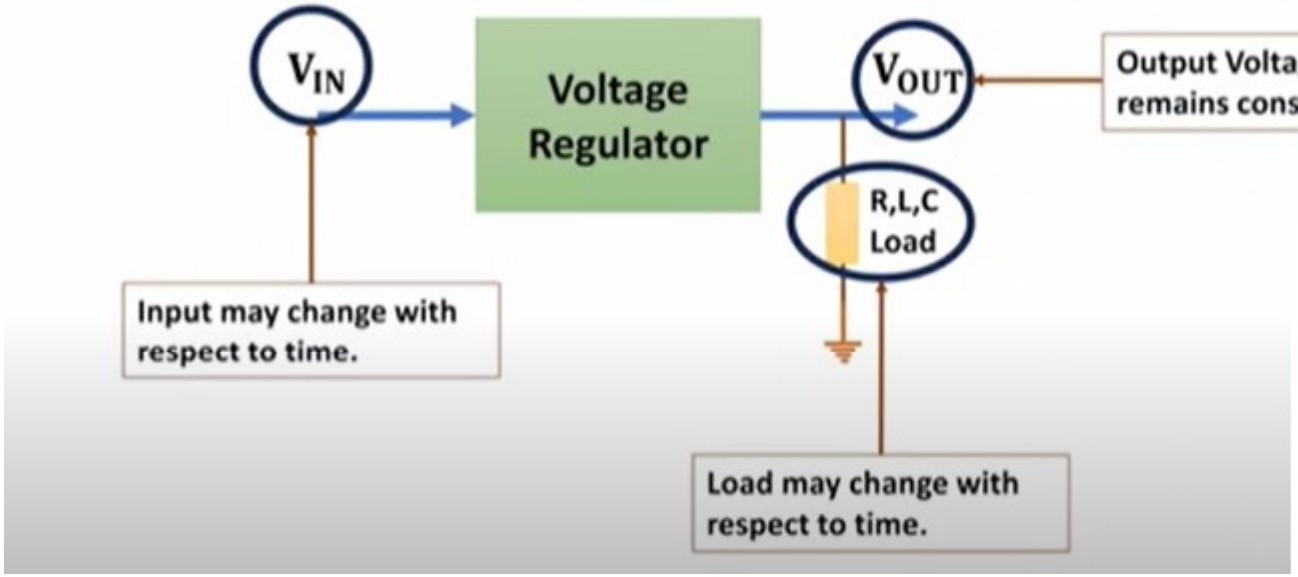


Fig. 9.14 PLL used as AM demodulator

Fixed Voltage Regulator ICs

Basics of Fixed Voltage Regulators

- It generates constant voltage regardless of changes in input voltage or load conditions.



Features of Fixed Voltage Regulators

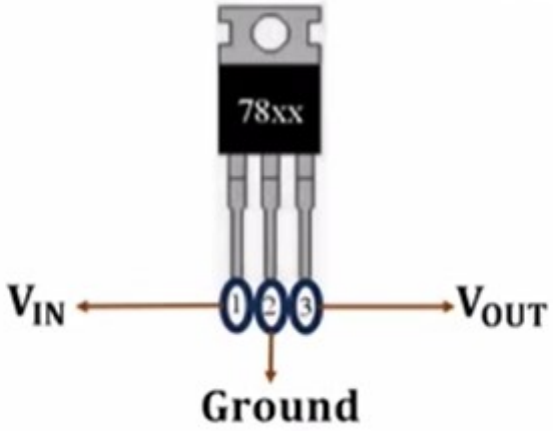
- Internal short circuit current limiting
- Thermal Shutdown
- Relatively inexpensive
- Programmable Output
- Current/Voltage Boosting

Fixed Voltage Regulators

- Positive Voltage Regulator
  - 7800 Series
  - Example: For 5 voltage regulation: 7805
  - Example: For 12 voltage regulation: 7812
- Negative Voltage Regulator
  - 7900 Series
  - Example: For -5 voltage regulation: 7905
  - Example: For -12 voltage regulation: 7912

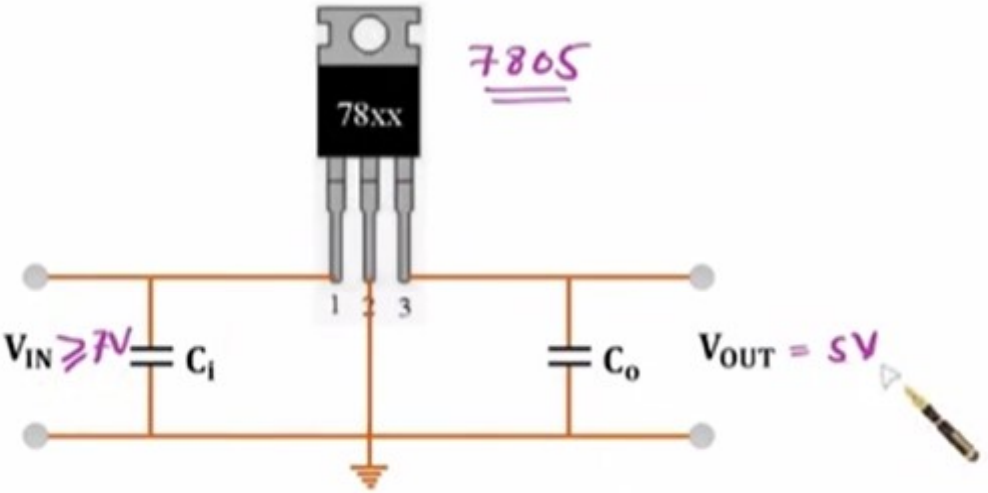
Positive Voltage Regulators

IC Number	Output Voltage	Maximum Input Voltage
7805	5V	35V
7806	6V	35V
7808	8V	35V
7812	12V	35V
7815	15V	35V
7818	18V	35V
7824	24V	40V



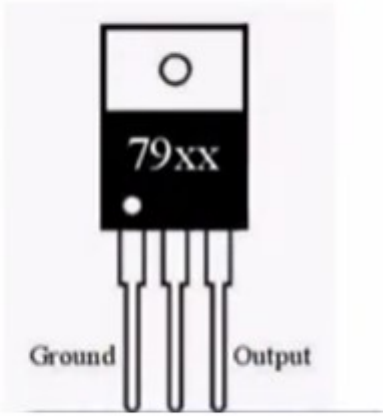
Conditions for proper operation of Positive Voltage Regulators

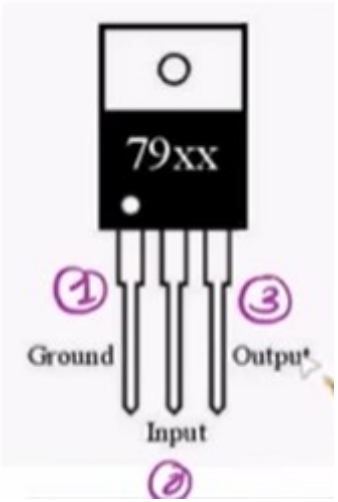
- Common Ground between input and output.
- Dropout voltage between input and output is 2V. So, $V_{IN} - V_{OUT} = 2V$
- C_i is required, if the regulator is located at considerable distance from power supply filter.
- C_o is not needed, it may be used to improve the transient response.



Negative Voltage Regulators

IC Number	Output Voltage	Maximum Input Voltage
7902	-2V	-35V
7905	-5V	-35V
7905.2	-5.2V	-35V
7906	-6V	-35V
7908	-8V	-35V
7912	-12V	-35V
7915	-15V	-35V
7918	-18V	-35V
7924	-24V	-40V

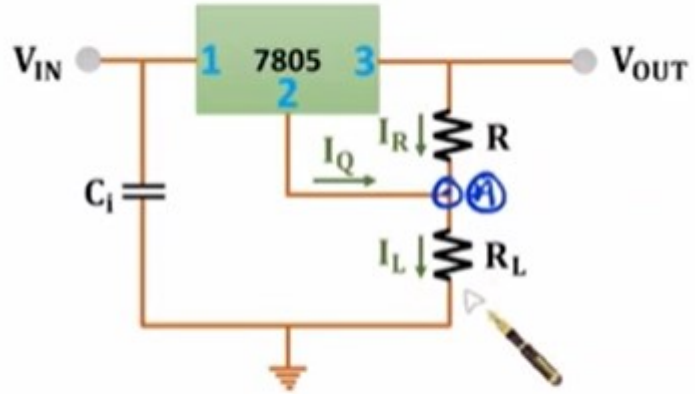




Performance Parameters of Voltage Regulators

- **Line Regulation**
  - It is a change in output for a change in input voltage.
  - It is expressed in millivolts or % of Output voltage.
  - Ideally, it should be zero.
- **Load Regulation**
  - It is a change in output voltage for a change in load current.
  - It is expressed in millivolts or % of Output voltage.
  - Ideally, it should be zero.
- **Temperature Stability**
  - It is a change in output voltage per unit change in temperature.
  - It is also called the average temperature coefficient of output voltage.
  - It is expressed in $\mathbf{mV/^0C}$.
  - Ideally, It should be zero
- **Ripple Rejection**
  - It is a measure of regulator's ability to reject ripple voltages.
  - It is expressed in dB.

Designing of Current Source using Voltage Regulator



↝ Apply KCL at Node (A)

$\Rightarrow I_L = I_R + I_Q$ — (1)

↑ It is Quiescent Current [with 7805, it is 5mA].

↝ $V_R = I_R R = 5V$

$\Rightarrow I_R = 5/R$ — (2)

↝ By substituting (2) into (1)

$\Rightarrow I_L = \frac{5}{R} + I_Q$

From the above equation load current is independent of load resistor

Question – Using a 7805 voltage regulator IC, design a current source that will deliver a 0.25A current to 48Ω, 10W load.

$\rightsquigarrow I_L = 0.25A$

$\rightsquigarrow I_L = \frac{5}{R} + I_Q$

$\Rightarrow 0.25 = \frac{5}{R} + 0.005$

$\Rightarrow 0.245 = \frac{5}{R}$

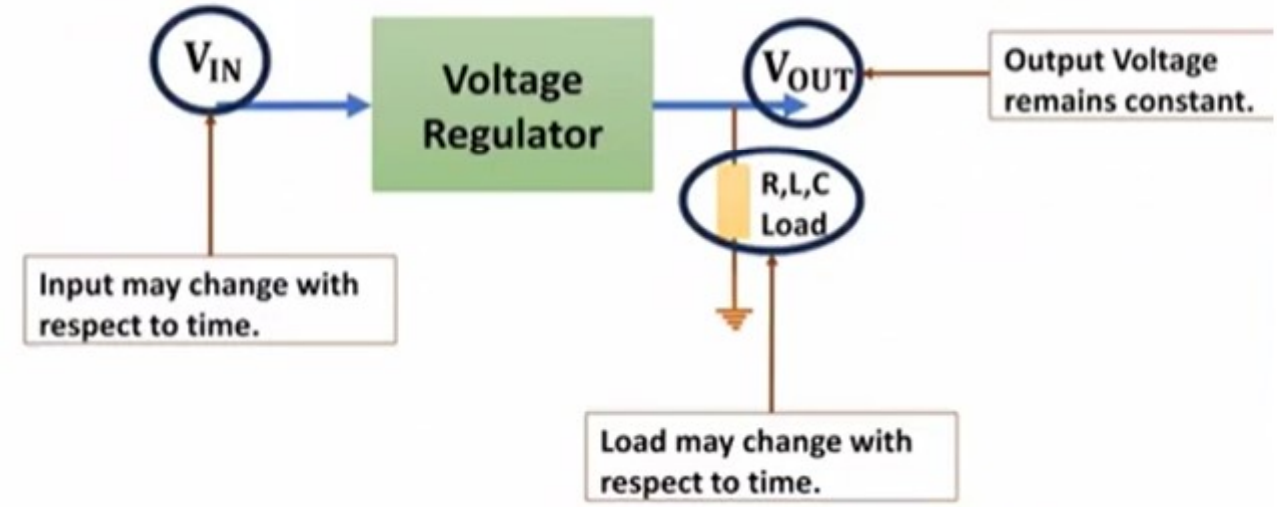
$\Rightarrow R = \frac{5}{0.245}$

$\Rightarrow R \approx 20\Omega$

Adjustable Voltage Regulator

Basics of Adjustable Voltage Regulators

- Fixed voltage regulator can regulate the voltage at a fixed voltage value at the output which leads to the following drawbacks:
  - Excessive Inventory
  - Production Cost
- Adjustable Voltage regulator can regulate the voltage at multiple voltage levels.



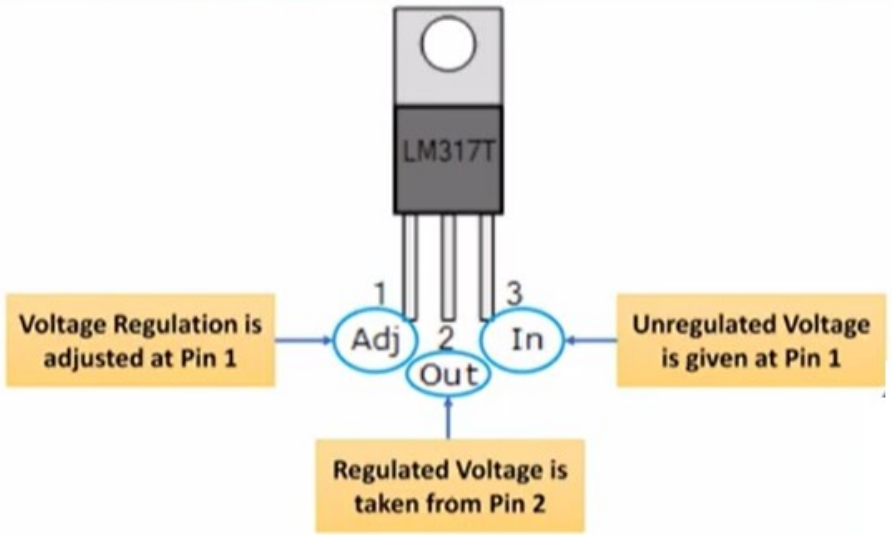
Advantages of Adjustable Voltage Regulators

- Single IC can regulate voltages from 1.2V to 37V.
- Better line and load regulation.
- Improved overload protection allows greater output current.
- Improved system reliability with each device being subjected to 100% thermal limit burn in.
- It reduces the inventory {In terms of numbers of different ICs} for production.
- Mass production results in lowering of cost.

Types of Adjustable Voltage Regulators

- Positive Adjustable Voltage Regulators
  - Example: LM317
- Negative Adjustable Voltage Regulators
  - Example: LM337

Pin Diagram of LM317 Positive Adjustable Voltage Regulator



Specifications of LM317 Positive Adjustable Voltage Regulator

IC	Output Range	Output Current	Vin Max
LM317	1.2V to 37V	1.5A	40V

Note:

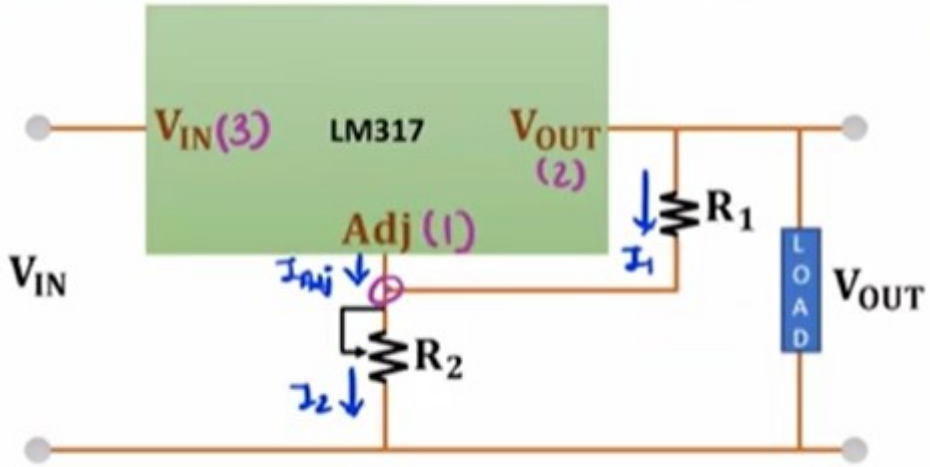
$$(V_{IN} - V_{OUT}) \leq 40V$$

$$(V_{IN} - V_{OUT}) \geq 3V$$

Minimum Dropout Voltage is 3V.

- With LM317, we have high power dissipation as we have a minimum 3V dropout voltage.
- Due to high power dissipation, with LM317, we need to have a power sink for the dissipation of power to avoid issues of circuit failure.

Circuit of LM317 Positive Adjustable Voltage Regulator

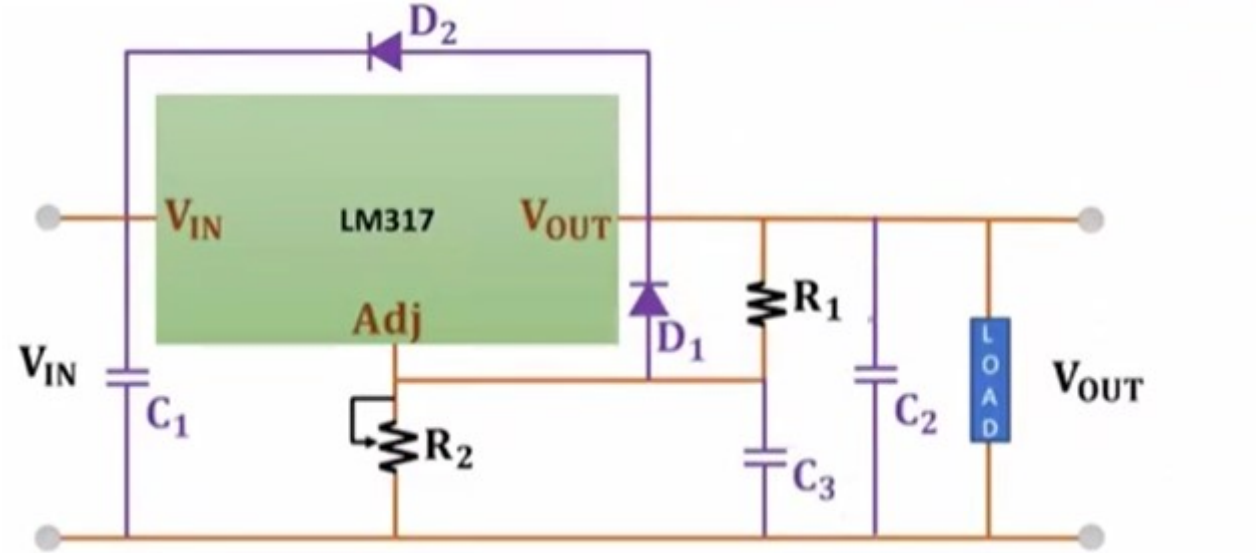


- With LM317, V_{REF} =1.25V develops in between Output and adjustable terminals.

$$\begin{aligned} V_{out} &= V_{R_1} + V_{R_2} \\ &= I_1 R_1 + I_2 R_2 \\ &= V_{Ref} + (I_1 + I_{Adj}) R_2 \\ &= V_{Ref} + \left(\frac{V_{Ref}}{R_1} + I_{Adj}\right) R_2 \\ &= \left(1 + \frac{R_2}{R_1}\right) V_{Ref} + I_{Adj} R_2 \end{aligned}$$

I_{Adj} = 100μA (for LM3

Modified adjustable voltage regulator with protection:



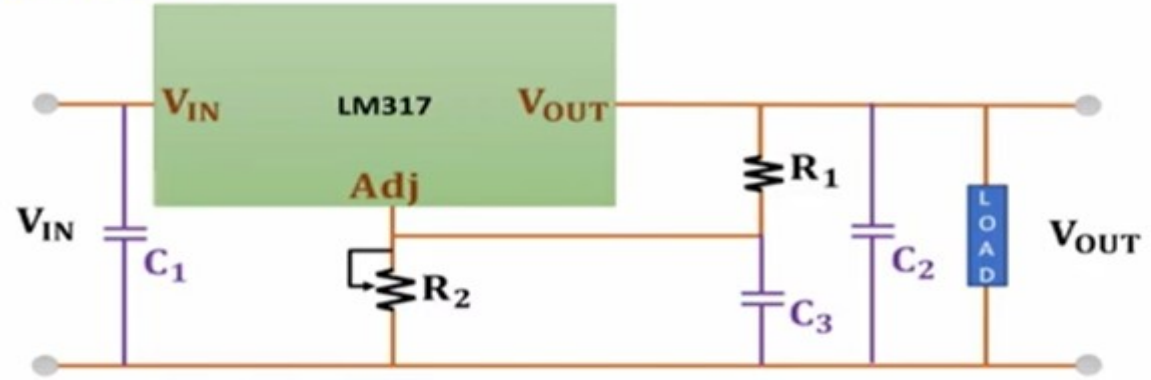
- C_1 is used when LM317 is situated far from the power supply.
- C_2 is optional to improve transient response.
- C_3 is bypass capacitor for adjustment terminal, it rejects ripple.
- D_1 and D_2 are protection diode to prevent capacitors from discharging through low current points. It is needed when output voltage is greater then 25V.
- Values of C_1, C_2, and C_3 should be lower then 25µF.

Question – Design an adjustable Voltage Regulator to satisfy the following specifications:

Output Voltage V_O = 5V to 12V

Output Current I_O = 1A

IC = LM317



$$\rightsquigarrow V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_{ref} + I_{Adj} R_2$$

$\rightsquigarrow$ For LM317, $V_{ref} = 1.25\,V$

$I_{Adj} = 100\,\mu A$

$$\Rightarrow V_{out} = \left(1 + \frac{R_2}{R_1}\right) 1.25 + 10^{-4} R_2$$

↝ Let us Assume $R_1 = 240\Omega$

⇒ $V_{out} = \left(1 + \frac{R_2}{240}\right) 1.25 + 10^{-4} R_2$

↝ V_{out} = 5V to 12V.

⇒ $5 = 1.25 + R_2\left(\frac{1.25}{240} + 10^{-4}\right)$

⇒ $\frac{3.75}{\left(\frac{1.25}{240} + 10^{-4}\right)} = R_2$

⇒ $R_2 = 706\,\Omega$

⇒ $12 = 1.25 + R_2\left(\frac{1.25}{240} + 10^{-4}\right)$

⇒ $\frac{10.75}{\left(\frac{1.25}{240} + 10^{-4}\right)} = R_2$

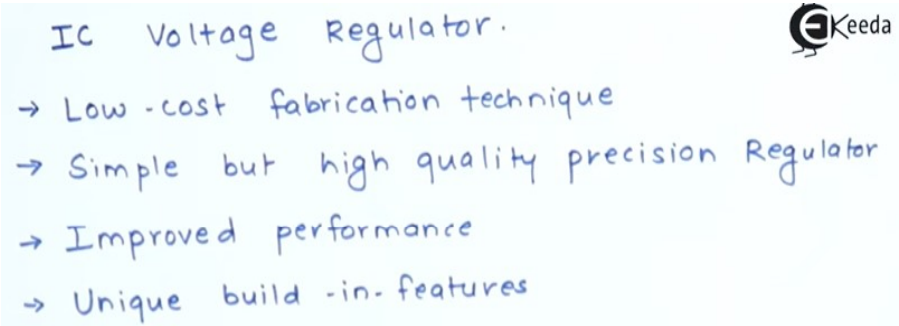
⇒ $R_2 = 2.02\,k\Omega$

Voltage regulator:

A voltage regulator is an integrated circuit (IC) that provides a constant fixed output voltage regardless of a change in the load or input voltage. It is a 3 pin IC.

The function of a **voltage regulator** is to maintain a constant DC voltage at the output irrespective of voltage fluctuations at the input and (or) variations in the load current. In other words, voltage regulator produces a regulated DC output voltage.

Types of Voltage Regulators:
There are **two types** of voltage regulators −
➢Fixed voltage regulator
1.Positive and 2. Negative
➢Adjustable voltage regulator:
1.Positive and 2. Negative



Fixed voltage regulator

A **fixed voltage regulator** produces a fixed DC output voltage, which is either positive or negative. In other words, some fixed voltage regulators produce positive fixed DC voltage values, while others produce negative fixed DC voltage values.

78xx voltage regulator ICs produce positive fixed DC voltage values, whereas, 79xx voltage regulator ICs produce negative fixed DC voltage values.

The following points are to be noted while working with **78xx** and **79xx** voltage regulator ICs –

"xx" corresponds to a two-digit number and represents the amount (magnitude) of voltage that voltage regulator IC produces.

Both 78xx and 79xx voltage regulator ICs have **3 pins** each and the third pin is used for collecting the output from them.

The purpose of the first and second pins of these two types of ICs is different −

The first and second pins of **78xx** voltage regulator ICs are used for connecting the input and ground respectively.

The first and second pins of **79xx** voltage regulator ICs are used for connecting the ground and input respectively.

Examples

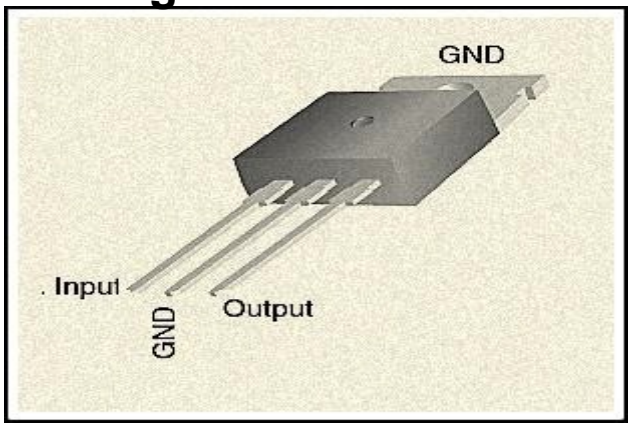
7805 voltage regulator IC produces a DC voltage of +5 volts.

7905 voltage regulator IC produces a DC voltage of -5 volts.

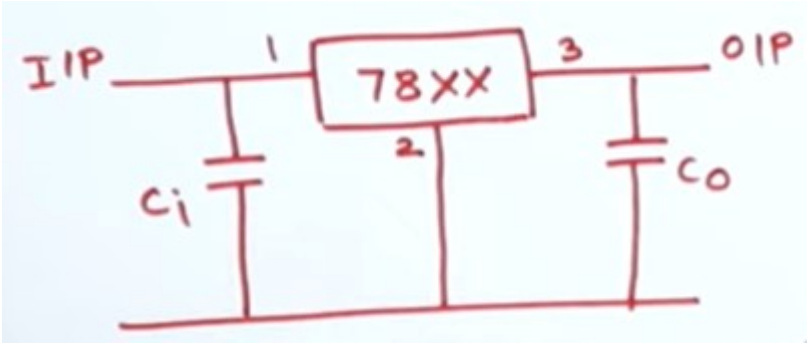
Fixed Positive voltage regulator

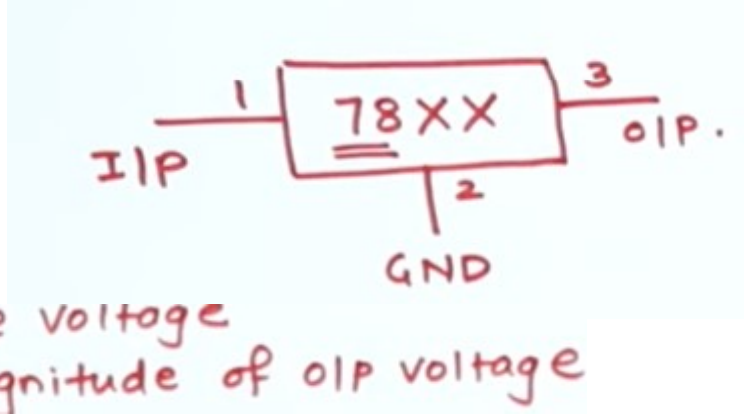
1. Fixed Positive voltage regulator
Pin diagram:
It is a 3 pin voltage regulator IC.
Pin 1: Input pin
Pin 2: Ground
Pin 3: output

Pin diagram:



Circuit diagram:





As per the pin diagram in the above circuit diagram input voltage is given to the pin-1, the output is taken from the pin-3 and the pin-2 is grounded. The positive voltage regulator provides positive voltage at its output. The best example for positive voltage regulator is 78xx IC. The last two digits or symbol 'xx' represent a level of voltage the can be produced at its output. For an example 7805 IC regulator provides constantly +5V at its output.

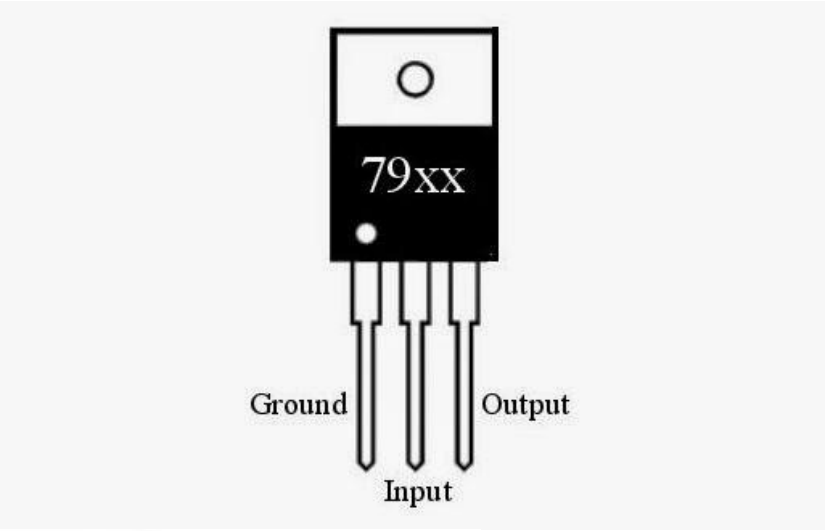
The types of ICs and its voltage ranges are given in the following table.

IC No	Voltage
7805	5V
7806	6V
7808	8V
7809	9V
7810	10V
7812	12V
7815	15V
7818	18V
7824	24V

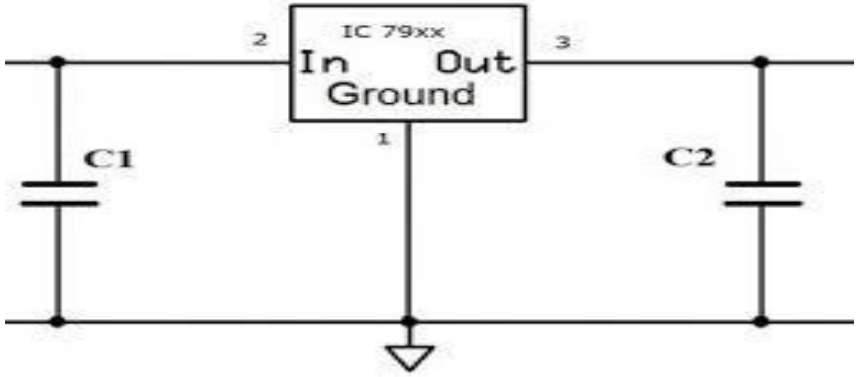
Fixed Negative voltage regulator

It is a 3 pin voltage regulator IC.

Pin 1: Ground
Pin 2: Input pin
Pin 3: output



Circuit dagram:



As per the pin diagram, in the above circuit diagram input voltage is given to the pin-2, the output is taken from the pin-3 and the pin-1 is grounded. The negative voltage regulator is same as the positive voltage regulator but the negative voltage regulator provides negative voltage at its output. The best example for negative voltage regulator is 79xx IC. The last two digits or symbol ‘xx’ represent the voltage level, for an example 7905 Ic regulator provides constantly -5V at its output.

The types of ICs and its voltage ranges are given in the following table.

Type number	Output voltage
7905	−5.0 V
7905.2	−5.2 V
7906	−6.0 V
7908	−8.0 V
7912	−12.0 V
7915	−15.0 V
7918	−18.0 V
7924	−24.0 V

The 7900 series

Performance Parameters of Voltage Regulators

1. Line Regulation : Change in output voltage for a change in the input voltage
   - expressed in millivolts or % of V_o

2. Load Regulation : Change in output voltage for a change in load current
   - expressed in millivolts or % of V_o

3. Temperature Stability : Average temperature Coefficient of o/p voltage

   Change in output voltage per unit change in temperature.
   - millivolts/°C

4. Ripple Rejection : Measure of regulator's ability to reject ripple voltages.

Adjustable voltage regulator

An adjustable voltage regulator produces a DC output voltage, which can be adjusted to any other value of certain voltage range. Hence, adjustable voltage regulator is also called as a **variable voltage regulator**.

The DC output voltage value of an adjustable voltage regulator can be either positive or negative.

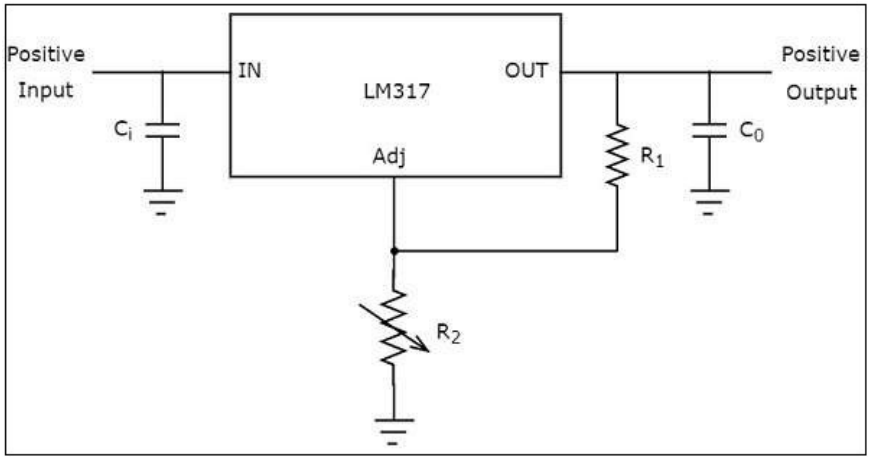
LM317 voltage regulator IC

LM317 voltage regulator IC can be used for producing a desired positive fixed DC voltage value of the available voltage range.

LM317 voltage regulator IC has 3 pins. The first pin is used for adjusting the output voltage, second pin is used for collecting the output and third pin is used for connecting the input.

The adjustable pin (terminal) is provided with a variable resistor which lets the output to vary between a wide range.

The figure shows an unregulated power supply driving a LM 317 voltage regulator IC, which is commonly used. This IC can supply a load current of 1.5A over an adjustable output range of 1.25 V to 37 V.



GENERAL PURPOSE REGULATOR USING LM 723

IC 723 voltage Regulator.

→ Series voltage Regulator. Provides +ve and -ve voltage.

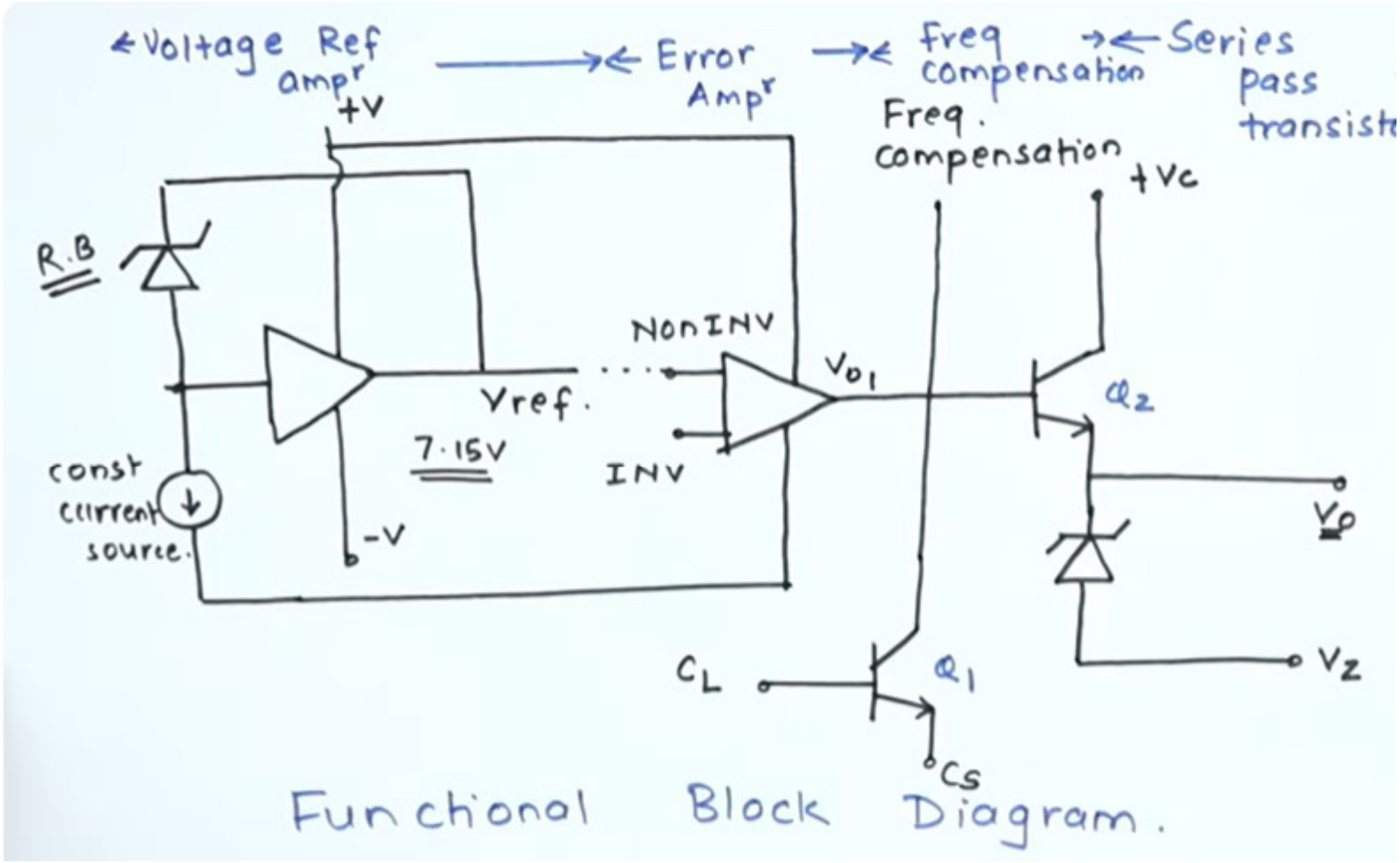
→ Provides current upto 150 mA. with external resistor current upto 10A

→ I/P voltage betⁿ 9 to 40V.

→ O/P voltage betⁿ 2 to 37V.

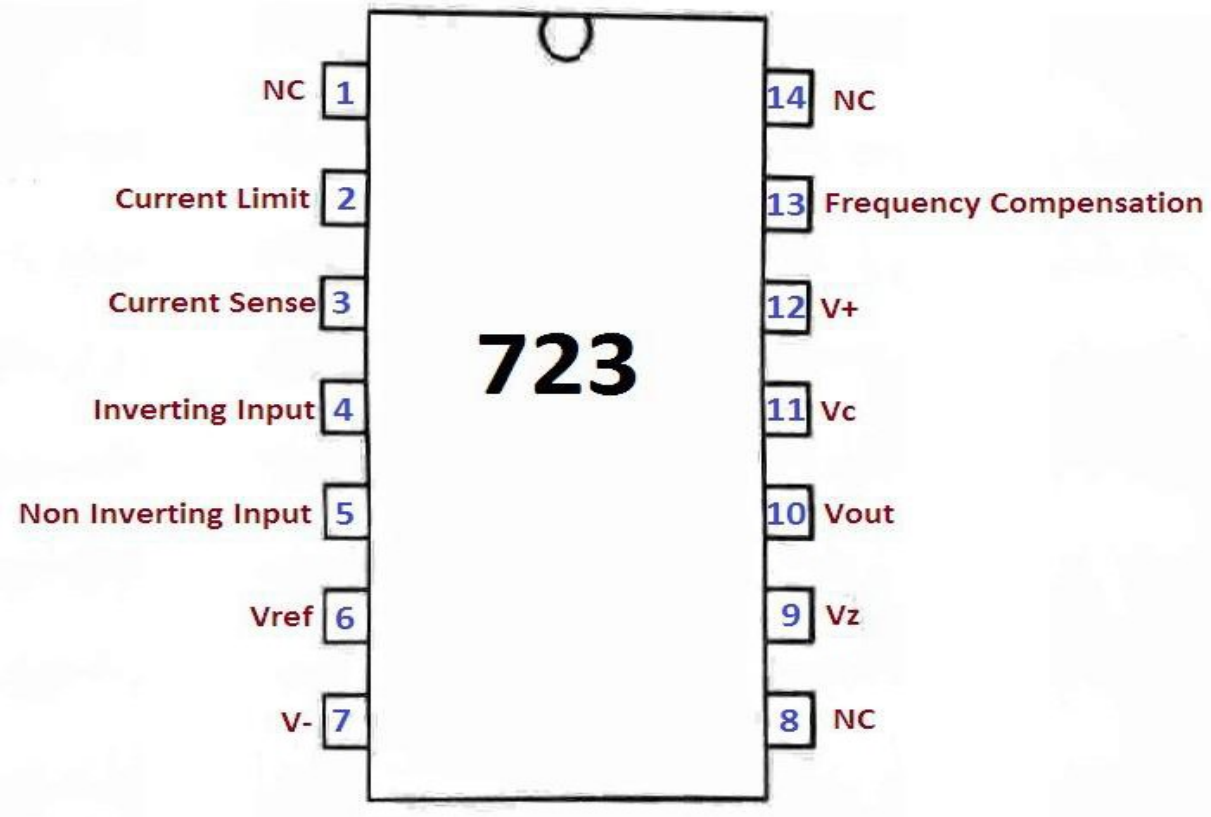
→ Load & Line regulation is 0.01%.

GENERAL PURPOSE REGULATOR USING LM 723



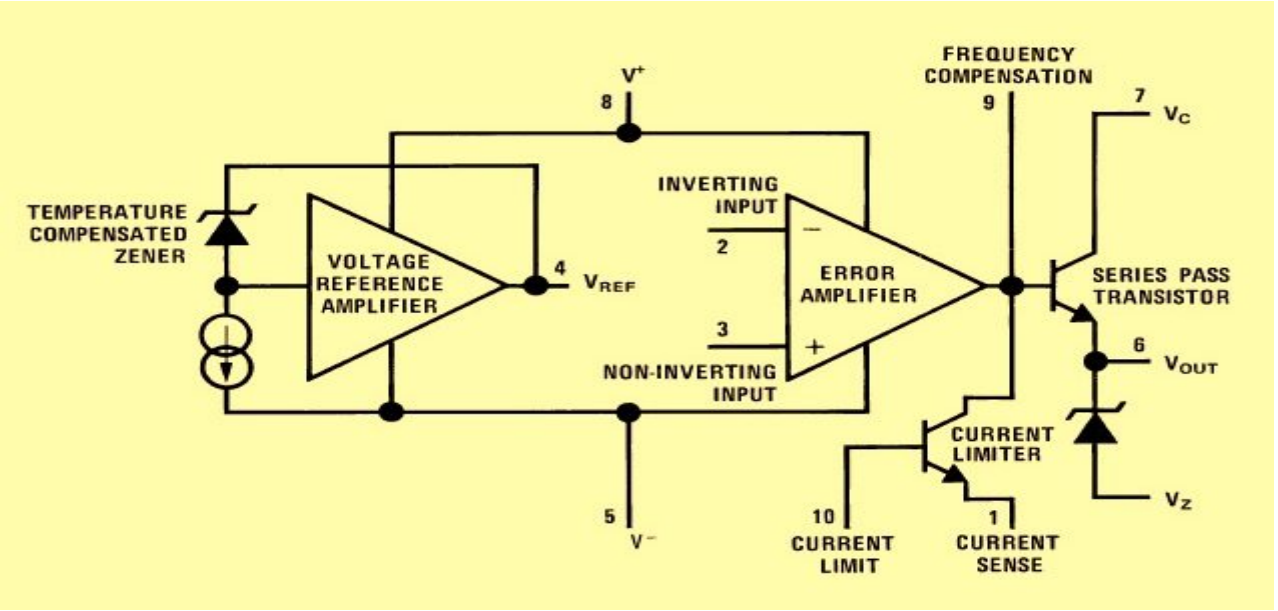
GENERAL PURPOSE REGULATOR USING LM 723

PIN DIAGRAM



It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both positive and negative voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels up to 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.

Internal Block Diagram



The internal working can be explained by dividing it into two blocks, the reference voltage generator and the error amplifier. In the reference voltage generator, a zener diode is being compelled to operate at fixed point (so that zener output voltage is a fixed voltage) by a constant current Source which comes along with an amplifier to generate a constant voltage of 7.15V at the Vref pin of the IC.

As for the error amplifier section, it consists of an error amplifier, a series pass transistor Q1 and a current limiting transistor. The error amplifier can be used to compare the output voltage applied at Inverting input terminal through a feedback to the reference voltage Vref applied at the Non-Inverting input terminal. These connections are not provided internally and so have to be externally provided in accordance with the required output voltage. The conduction of the transistor Q1 is controlled by the error signal. It is this transistor that controls the output voltage.

D/A AND A/D CONVERTERS

Naturally, physical quantities such as voltage, current, pressure & temperature signals are in analog form. It is very difficult for real time applications and to store the signals.

To solve the above problems the analog signal should be converted into digital form. It gives accuracy, speed & better performance.

In the transmitter side the analog signal has to be converted into digital form & the necessary process takes place within the computer.

After completion of the process within the system, it should be again converted into the original form at the receiver side i.e., analog form. So, for a complete system Analog to Digital & Digital to Analog conversion is necessary.

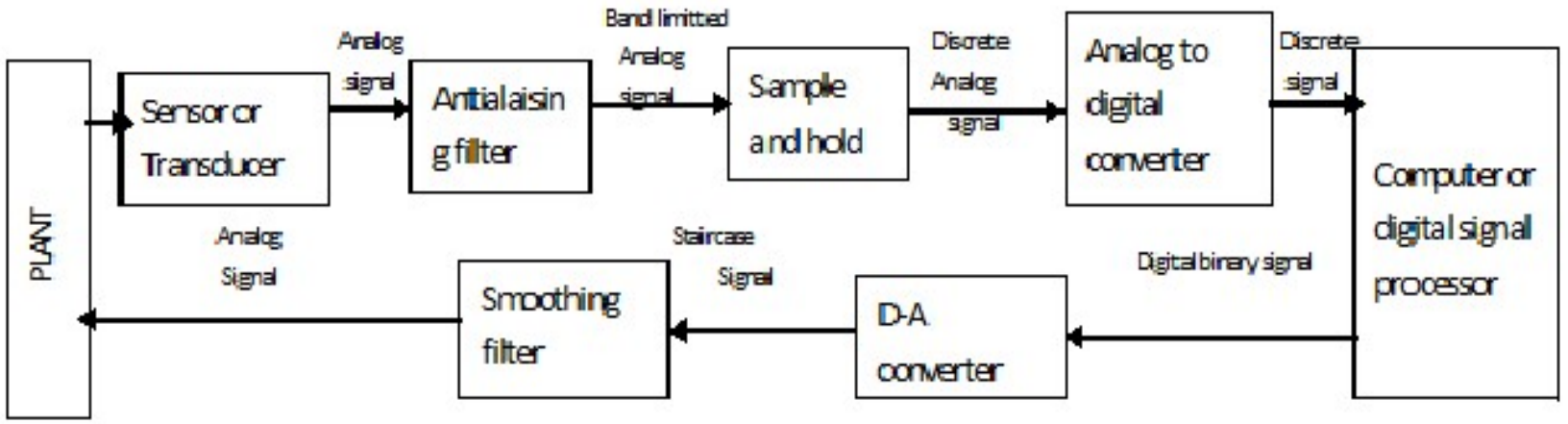
The basic building block diagram of Analog to Digital & Digital to Analog conversion is shown below:

It has 2 main parts namely,
1) Analog to Digital conversion 2) Digital to Analog conversion

Why Analog to Digital ?

- In real world, the physical quantities like voltage, current, temperature, pressure and time are available in analog form.
- It is difficult to store, process & transmit the analog signals.
- Affects with noise.
- The digital signals can easily store, process & transmit.

BLOCK DIAGRAMOF ADC & DAC



Analog to Digital conversion:

The sensor & transducer connects the input analog signal to the Analog to Digital converter & it converts the non electrical input signal into electrical signal.

Antialiasing filter is used before a signal sampler to restrict the bandwidth of a signal to satisfy the Nyquist rate, band limit the analog signal i.e., there by band width requirement is reduced.

Sample & hold circuit is used to sample the band limited signal based on the sample theorem. So the signal becomes a discretized signal. Though the signal is in analog form, hold the discrete signal until the conversion is completed.

Analog to Digital converter converts the discretized signal into binary digits i.e., discrete digital signal and then it is given to the processors.

Digital to Analog conversion:

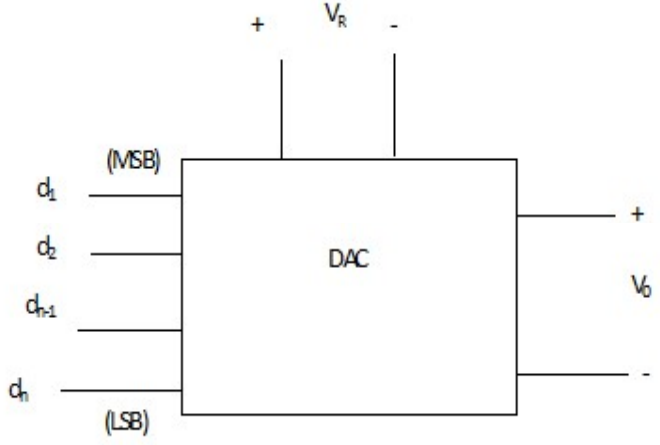
Digital to Analog conversion is just the reverse process of Analog to Digital conversion.

The digital data is again reconverted back into analog by doing exact opposite operation of first half of the diagram. Then the output of the D/A convertor is transmitted through the smoothing filter to avoid the ripples.

BASIC STRUCTURE OF DAC

It has i) Digital to Analog converter

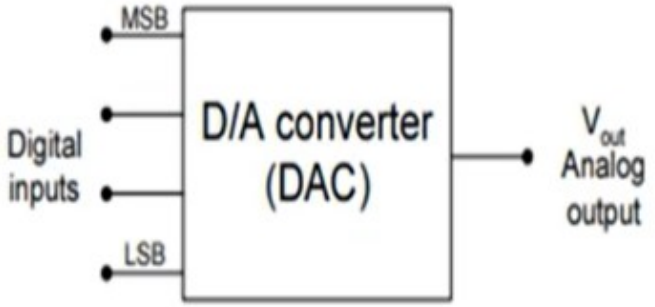
ii) Smoothing filter.



Digital to Analog converter is used to convert the digital binary bits into analog signal. But Analog to Digital converter & Digital to Analog converters are operated at same frequency. The Digital to Analog converter produces a staircase output & which is given to the smoothing filter.

The smoothing filter is used to convert the stair case signal to the smooth analog signal. Also the smoothing filter reduces the quantization noise. Analog to Digital & Digital to Analog converter is designed in same circuit i.e., a circuit that can act as an Analog to Digital & Digital to Analog converter is called Data converter & it is also available in the form of integrated chip IC.

Digital to Analog Converters

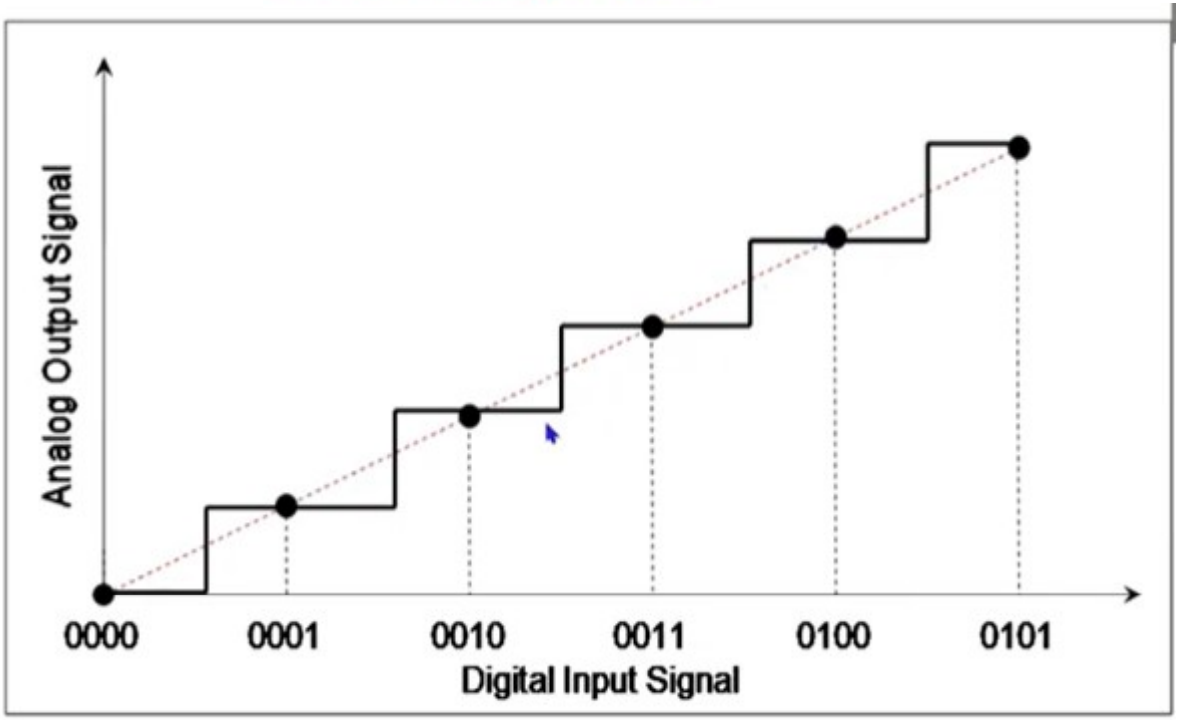


- A DAC accepts an n-bit input word b1,b2,b3,...bn in binary and produce an analog signal proportional to it.
- Ex: 1 0 1 0 1 1
- LSB: Least Significant Bit
- MSB: Most Significant Bit
- The output of DAC cab be either a voltage or current.
- For voltage output the output expression is :

$$V_o = K V_{FS} (D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} + ... + D_n 2^{-n} \rightarrow (1)$$

- Where, Vo = output voltage
- V_{FS}= Full scale output voltage
- K = scalling factor usually adjusted to unity
- D1 , D2 ...Dn = n-bit fractional word.
- D1 = MSB
- Dn = LSB

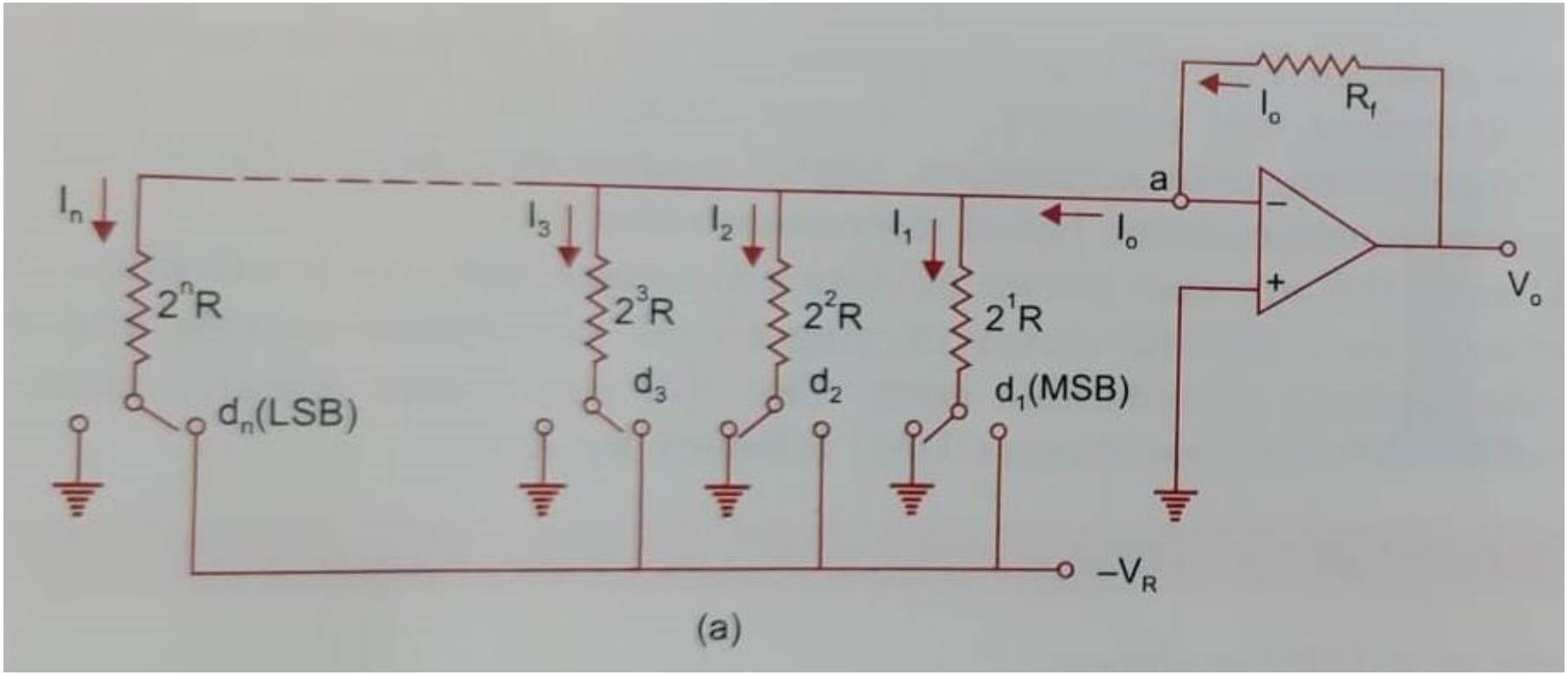
DAC Response:



TYPES OF DAC : DACs are implemented by switches, resistors, op-amps

- Many types of DACs available.
- Usually switches, resistors, and op-amps used to implement conversion
- Two Types:
  - Binary Weighted Resistor
  - R-2R Ladder

WEIGHTED RESISTOR:

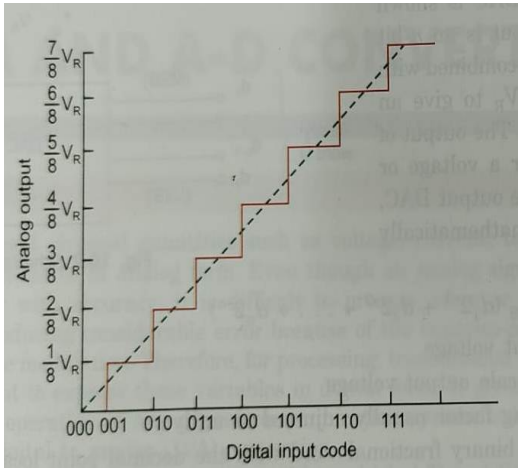


Weighted Resistor DAC uses summing amplifier with binary weighted resistor network.

It consists of: i) Summing amplifier ii) Different ranges of resistor iii) Electronic switches.

It has n electronic switches d1, d2, d3.....dn controlled by binary input word. These switches are single pole double throw(SPDT) type.

If the binary input to a particular switch is '1', it connects the resistance to the reference voltages (- V_R).
If input bit is '0', switch connects the resistor to the ground.



Transfer Characteristics of 3 bit DAC

If the output current I_0 for Ideal op amp can be written as:

$$I_0 = I_1 + I_2 + I_3 + \ldots\ldots\ldots + I_n$$

$$I_Q = \frac{V_R\, d_1}{2^1 R} + \frac{V_R\, d_2}{2^2 R} + \ldots\ldots\ldots \frac{V_R\, d_n}{2^n R}$$

$$= \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}\right)$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}\right) \qquad (10.2)$$

Comparing Eq. (10.1) with Eq. (10.2), it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 10.3 (a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 10.3 (b) for a 3-bit weighted resistor DAC. It may be noted that

Disadvantages: 1) Wide range of resistors is needed. 2) If number of bits increases, then number of resistors and switches also increases. 3) If the word length increases, then the circuit becomes complex.

R-2R LADDER DAC

Wide range of resistors required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC.

But the vital problem in weighted register D/A converter is use of huge range of different resistance.

So the largest resistor corresponding to bit b8 is 128 times the value of the smallest resistor correspond to b1. But in case of R-2R ladder D/A converter,

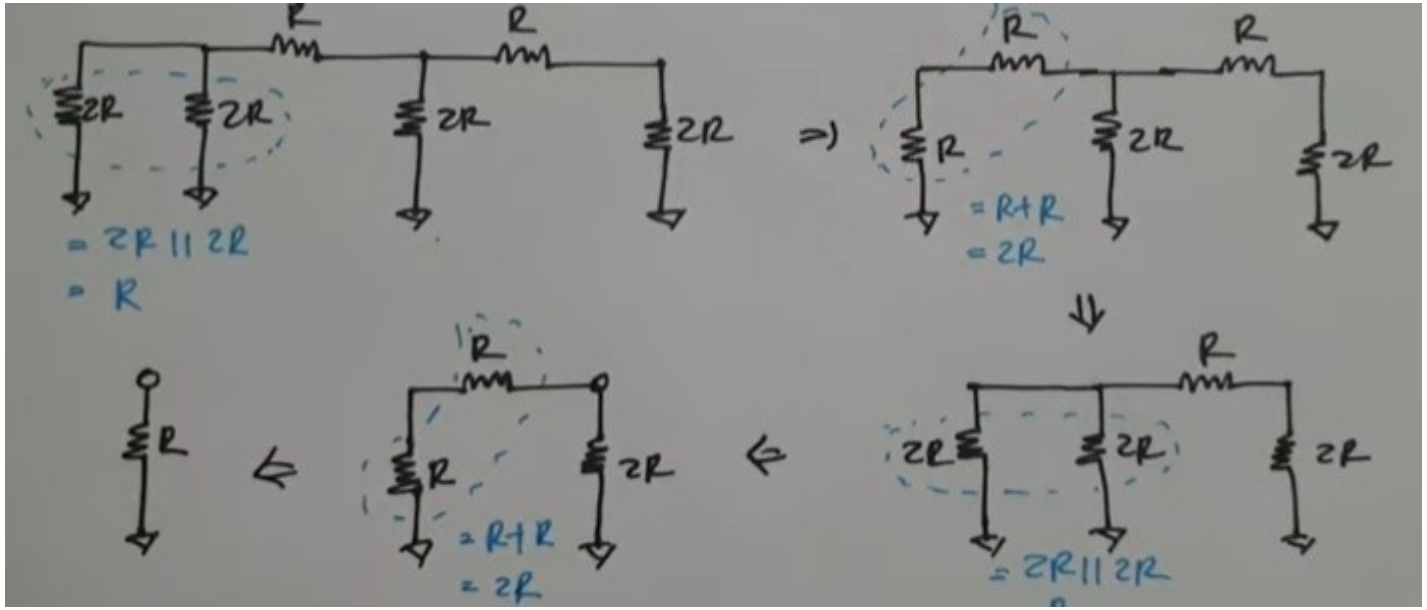
Resistors of only two values (R and 2R) are used. Now in bellow see the simple ladder network.

In ladder circuit the output voltage is also weighted sum of the corresponding digital input.

- A Digital to Analog Convertor is used when the binary output from a digital system is to be converted into its equivalent analog voltage or current.
- This type of converter has only two values of resistors R and 2R. The conversion speed reduces in this type due to parasitic capacitance. It is the simplest type o DAC where the switch between ground and inverting input of the op-amp is controlled by the input bit.

Advantages: Impedance of resistive network is constant i.e: R, so accurate output produced

1] It uses only two Values of Resistor. Hence easy and accurate fabrication can be done.
2] It is easy to Scale with respect to number of bits.
3] Impedence of Network is R, regardless of number of bits.



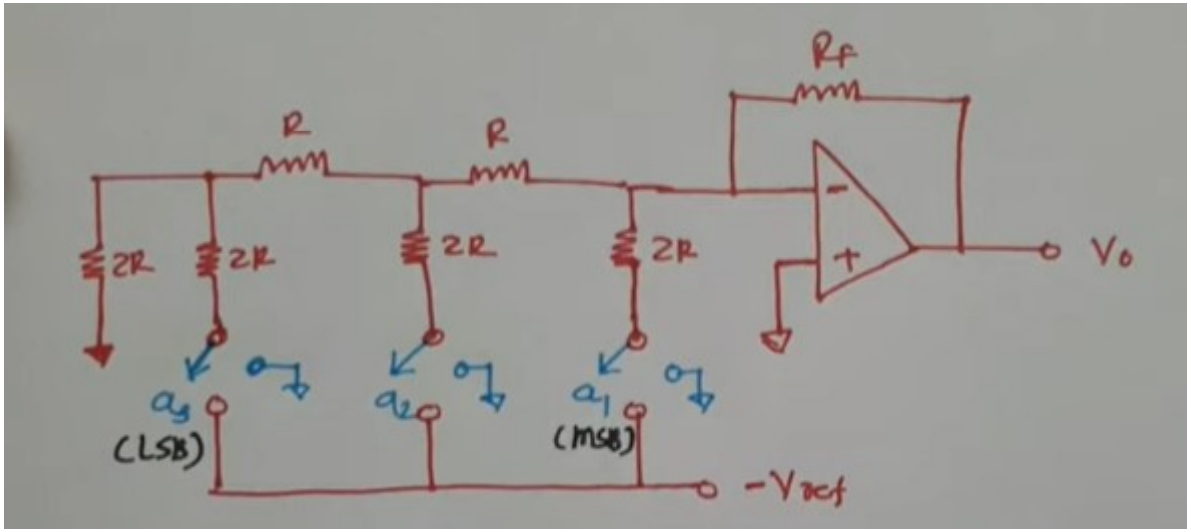
From the above analysis impedance of network is R, it not depend on number of bits. If increase no.of bits the network impedance not changed.

3-bit DAC shown in fig. Where Switch position d1d2d3 corresponds to the binary word 100.

The circuit can be simplified to the equivalent circuit (b).

The voltage at C can be calculated by network analysis as

3-bit DAC:(voltage switched)

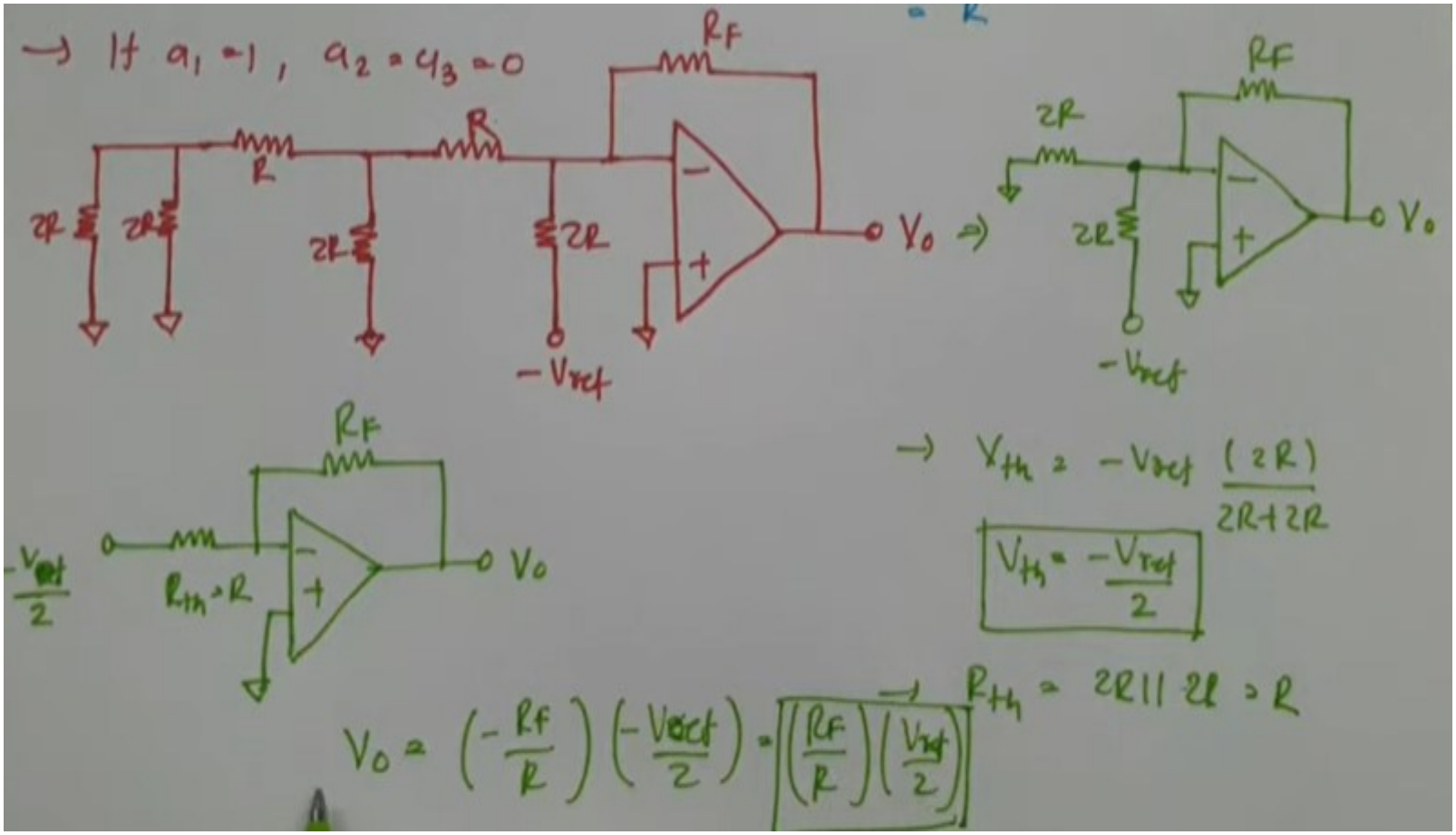


$$V_0 = \left(\frac{R_f}{R}\right) V_R \left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8}\right)$$

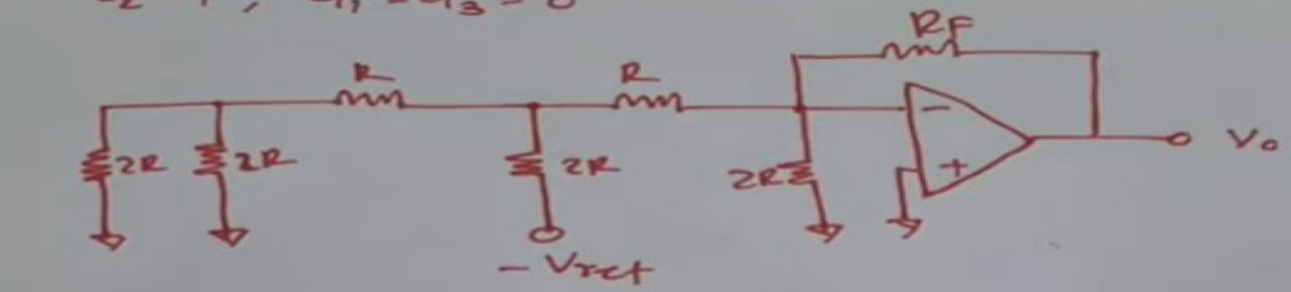
Where a1,a2, a3 are binary digits

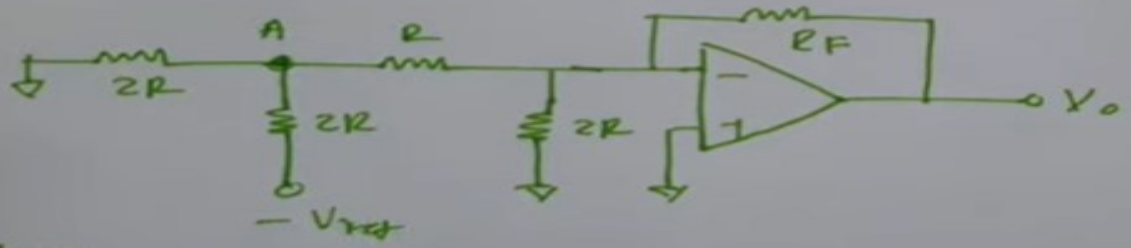
Working:

- This uses Kirchhoff's current law, which states that the sum of currents entering a node must be equal to the sum of currents leaving a node.
- In the ladder, at each node, the current is split in half. By switching the currents into each node, the total current flowing is binary weighted.
- Using the principle of superposition, when you add more current into a resistance the total voltage appearing is the sum of the voltages caused by all the individual currents i.e. as each bit is activated, so the voltage increases at the output. This results in the conversion of the input digital stream in analog value.

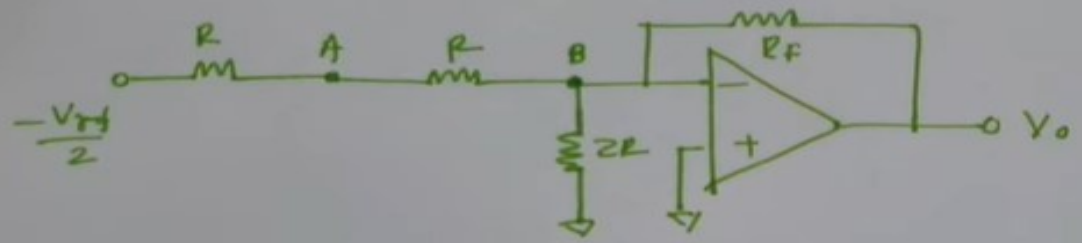

→ If $a_1 = 1$, $a_2 = a_3 = 0$
R_F
R
R
2R
2R
2R
2R
V_o
$-V_{ref}$
$\Rightarrow$
R_F
2R
2R
V_o
$-V_{ref}$
R_F
$\frac{-V_{ref}}{2}$
$R_{th} = R$
V_o
$\rightarrow V_{th} = -V_{ref} \frac{(2R)}{2R+2R}$
$V_{th} = -\frac{V_{ref}}{2}$
$\rightarrow R_{th} = 2R \| 2R = R$
$V_o = \left(-\frac{R_F}{R}\right)\left(-\frac{V_{ref}}{2}\right) = \left(\frac{R_F}{R}\right)\left(\frac{V_{ref}}{2}\right)$

→ $a_2 = 1$, $a_1 = a_3 = 0$

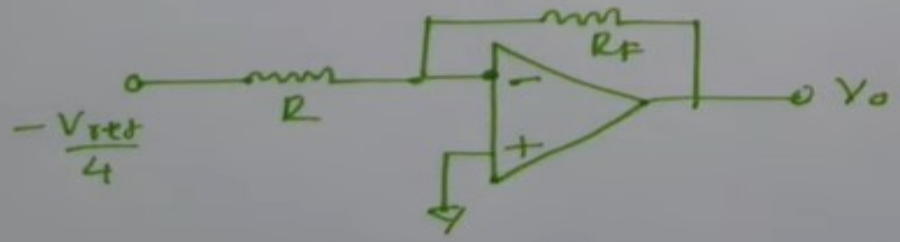




at A, $V_{th} = \dfrac{-V_{ref}(2R)}{2R+2R} = -\dfrac{V_{ref}}{2}$, $R_{th} = 2R \,||\, 2R = R$



- at B, $V_{th} = \dfrac{\left(-\frac{V_{ref}}{2}\right)(2R)}{2R+2R} = -\dfrac{V_{ref}}{4}$, $R_{th} = 2R \,||\, 2R = R$

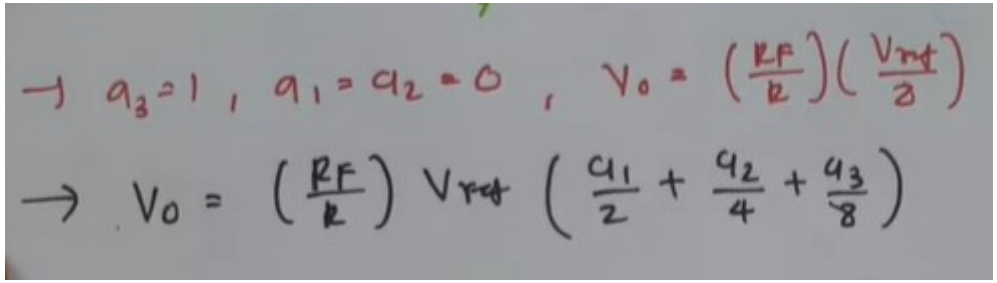


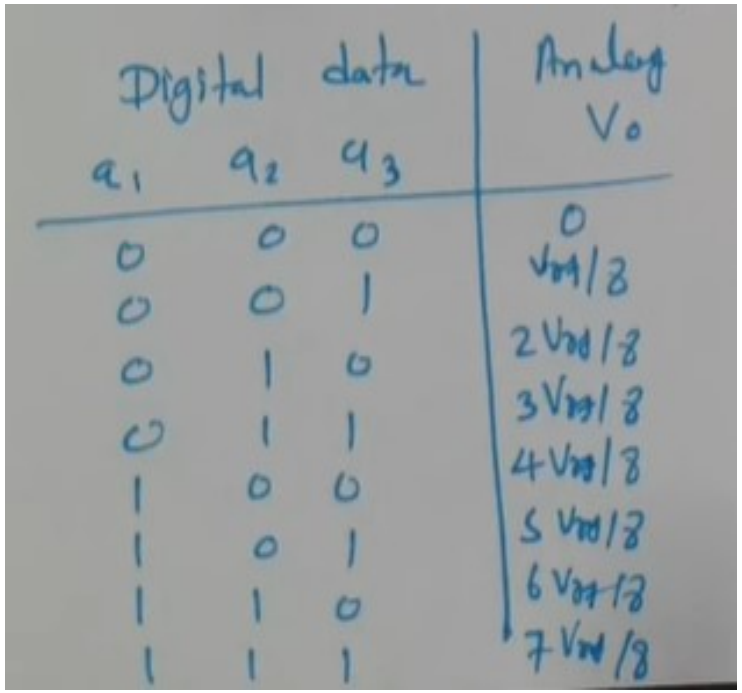
$$V_o = \left(-\frac{R_F}{R}\right)\left(-\frac{V_{ref}}{4}\right)$$

$$= \left(\frac{R_F}{R}\right)\left(\frac{V_{ref}}{4}\right)$$

If

Output voltage





Digital data			Analog V_o
q_1	q_2	q_3	
0	0	0	0
0	0	1	$V_{ref}/8$
0	1	0	$2V_{ref}/8$
0	1	1	$3V_{ref}/8$
1	0	0	$4V_{ref}/8$
1	0	1	$5V_{ref}/8$
1	1	0	$6V_{ref}/8$
1	1	1	$7V_{ref}/8$

Applications:

- Audio Amplifier
- Video Encoder
- Display Electronics
- Data Acquisition Systems
- Motor Control
- Software Radio, etc..

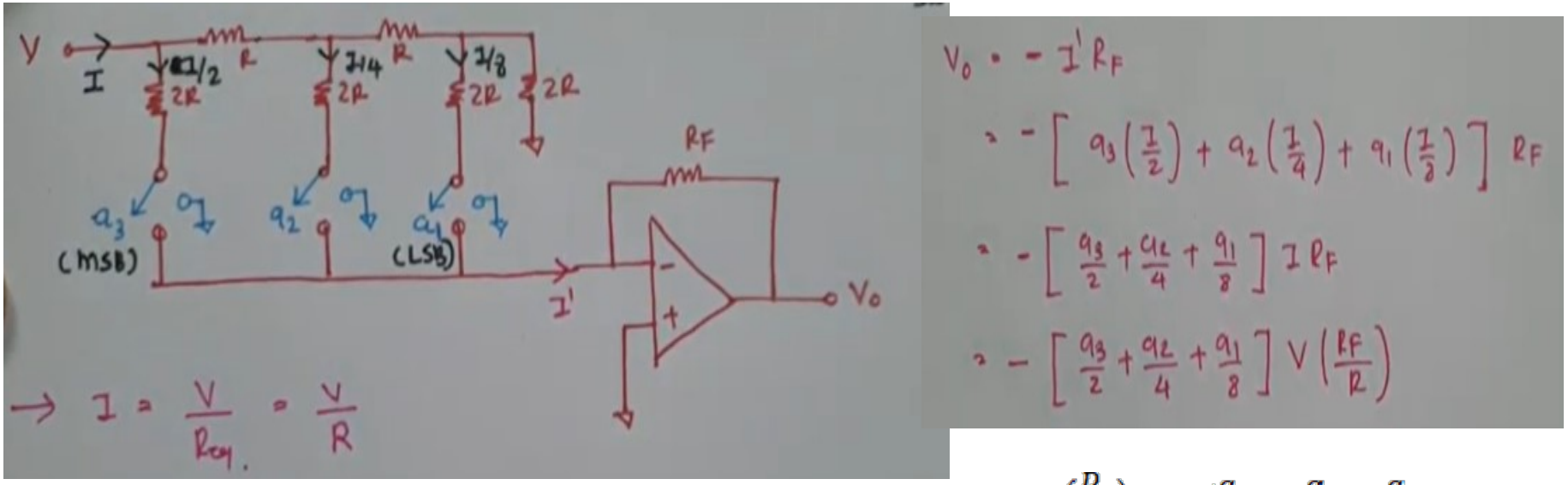
Working:

- This uses Kirchhoff's current law, which states that the sum of currents entering a node must be equal to the sum of currents leaving a node.
- In the ladder, at each node, the current is split in half. By switching the currents into each node, the total current flowing is binary weighted.
- Using the principle of superposition, when you add more current into a resistance the total voltage appearing is the sum of the voltages caused by all the individual currents i.e. as each bit is activated, so the voltage increases at the output. This results in the conversion of the input digital stream in analog value.

INVERTED R-2R LADDER DAC (current switched)

In weighted resistor and R-2R ladder DAC the current flowing through the resistor is always changed because of the changing input binary bits 0 and 1. More power dissipation causes heating, which in turn cerates non-linearity in DAC. This problem can be avoided by using INVERTED R-2R LADDER DAC .

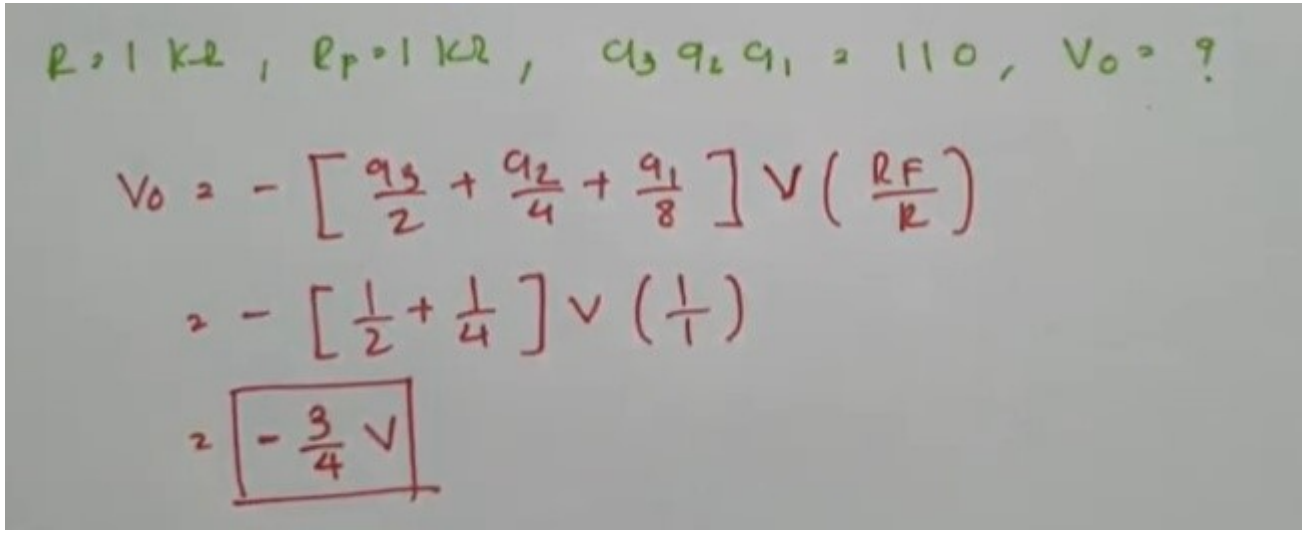
In this MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of op-amp which is also at virtual ground. When the input binary in logic 1 then it is connected to the virtual ground, when input binary is logic 0 then it is connected to the ground
i.e. the current flowing through the resistor is constant.



INVERTED R-2R output voltage $V_0 = -\left(\frac{R_f}{R}\right) V \left(\frac{a_3}{2} + \frac{a_2}{4} + \frac{a_1}{8}\right)$

Find output voltage for R-2R ladder DAC, if Rf =1k, R=1K, and a3a2a1=110

$$V_0 = -\left(\frac{R_f}{R}\right) V \left(\frac{a_3}{2} + \frac{a_2}{4} + \frac{a_1}{8}\right)$$



Resolution: The minimal possible change at the output of DAC for any change in digital input

Resolution = Step size in volts = (LSB value) = $V_R / 2^N$ = Full scale voltage(FSV) / (2^N-1)

% Resolution = (Step Size /FSO) *100= (Step Size / (2^N-1) X Step Size *100= $(100/ 2^N-1)$

Full scale output voltage =(2^N-1) X Step Size =V_R – weight of LSB

Number of steps = Vin / resolution

Output Voltage of n bit DAC = Resolution X Binary equivalent of digital input

output voltage

Example 1: In R-2R DAC. Find the full scale output voltage if Rf=2K, R=1K. Also find output voltage when the input is 10110. Assume Vref=5V, find resolution & Full scale range.

output voltage $V_0 = -V_{ref}\left(\frac{R_f}{R}\right)\left(\frac{a_1}{2} + \frac{a_2}{4} + \frac{a_3}{8} + \frac{a_4}{16} + \frac{a_5}{32}\right)$

- For Full scale output, $a_1a_2a_3a_4a_5 = 11111$

$$V_0 = -5\left(\frac{2}{1}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$$
$$= -10\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$$
$$= -10\left(\frac{16+8+4+2+1}{32}\right)$$
$$= -10\left(\frac{31}{32}\right) = -9.6875 \text{ Volt}$$

- For Input $a_1a_2a_3a_4a_5 = 10110$

$$V_0 = -5\left(\frac{2}{1}\right)\left(\frac{1}{2} + \frac{1}{8} + \frac{1}{16}\right)$$
$$= -10\left(\frac{8+2+1}{16}\right)$$
$$= -10\left(\frac{11}{16}\right) = -6.875 \text{ Volt}$$

- Resolution (step size) $= K\frac{V_{ref}}{2^n}$

$$= \left(\frac{R_f}{R}\right)\left(\frac{V_{ref}}{2^n}\right)$$
$$= \left(\frac{2}{1}\right)\left(\frac{5}{2^5}\right) = \frac{10}{32} = 0.3125 \text{ Volt}$$

- Full scale Range $= V_{ref}\left(\frac{R_f}{R}\right)\frac{(2^n-1)}{2^n}$

$$= 5\left(\frac{2}{1}\right)\frac{(2^5-1)}{2^5}$$
$$= 10\left(\frac{31}{32}\right)$$
$$= 9.6875 \text{ Volt.}$$

Find the Vmax & Vmin for 11111 Input with binary weighted DAC. $V_{ref} = 10\ V$, $R_F = R = 1\ K\Omega$, Resistance tolerance 2%. Also Find Resolution, Full Scale Voltage.

→ $V_o = -V_{ref}\left(\frac{R_F}{R}\right)\left(\frac{q_1}{2} + \frac{q_2}{4} + \frac{q_3}{8} + \frac{q_4}{16} + \frac{q_5}{32}\right)$

$= -10\left(\frac{1}{1}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$

$= -10\left(\frac{16+8+4+2+1}{32}\right)$

$= -10\left(\frac{31}{32}\right) = -9.6875$ Volt.

→ For Vmax, $R_F = 1.02\ K\Omega$, $R = 0.98\ K\Omega$, $q_1q_2q_3q_4q_5 = 11111$

$V_{o_{max}} = -10\left(\frac{1.02}{0.98}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$.

$= -10.0829$ Volt

$= -10.0829$ Volt

→ For Vmin, $R_F = 0.98\ K\Omega$, $R = 1.02\ K\Omega$, $q_1q_2q_3q_4q_5 = 11111$

$V_{o\,min} = -10\left(\frac{0.98}{1.02}\right)\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32}\right)$

$= -9.30759$ Volt

→ Resolution $= K\frac{V_{ref}}{2^n} = \left(\frac{R_F}{R}\right)\frac{10}{2^5}$

$= \frac{10}{25} = 0.3125$ Volt

$FSV = V_{ref}\frac{(2^n - 1)}{2^n}$

$= 10\left(\frac{2^5 - 1}{2^5}\right)$

$= 10\left(\frac{31}{32}\right) = 9.6875$ Volt

A **10-bit** DAC has a step size of 10 **mV**. What is its Full scale O/P voltage and the **percentage resolution**? What is output voltage for an input is 1011001101

Resolution = Step size in volts = (LSB value) = $V_R / 2^N$ = Full scale voltage(FSV) / (2^N-1)

Given n = 10 bits

$$FSO\ (V_{FS}) = (2^N - 1) \times step\ size$$

$VFS = (1023) \times 10 \times 10^{-3} = 10.23\ V$

$V_{FS} = 10.23\ V$

$$R = \frac{10.23}{2^{10}-1} \times 100$$

R = 1%

An 8-bit DAC has a resolution of 20 mV/LSB. Find V_0 if the input is $(10000000)_2$.

Concept:

The output for an 'n' bit DAC is given by:

V_o = Resolution × (Binary equivalent of digital input)

The resolution is obtained by:

$$R = \frac{V_{ref}}{2^n}$$

Given, resolution = 20 mV/LSB

The binary equivalent of the digital input is:

$(10000000)_2 = 1 \times 2^7 = 128\ V$

$V_o = 20 \times 10^{-3} \times 128$

V_o = 2.56 V

Problem:

- Suggest the values of resistors and reference voltage if resolution required is 0.5 V for 4 bit R/2R ladder type DAC.

$$\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R}\right) \times R_f$$

Let $V_R = 10\ V$, $n = 4$ and resolution $= 0.5$

$$\therefore \quad 0.5 = \frac{1}{2^4} \times \frac{10}{R} \times R_f$$

$$\therefore \quad \frac{R}{R_f} = 1.25$$

Choose $R_f = 10\ k\Omega$ | $R = 12.5\ k\Omega$

Problems:

- The LSB of a 10-bit DAC is 20 m volts.
  (i) What is its percentage resolution?
  (ii) What is its full-scale range?
  (iii) What is the output voltage for an input, 10110 01101?

Solution : i) $20 \times 10^{-3} \times 100 = 2\ \%$

$V_{oFS} = (2^n - 1) \times \text{Resolution} = 20.46\ V$

ii) $(101100\ 1101)_2 = 717$

$V_o = 717 \times 20 \times 10^{-3}$

$= 14.34\ V$

SPECIFICATIONS OF DAC: Specifications of DAC are
1. Accuracy 2. Resolution 3. Monotonocity 4. Settling time.

Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.

Resolution: It can also be defined as the ratio of change in analog output voltage resulting from a change of 1LSB at the digital input.
For n-bit DAC, Resolution=VFS (2n−1) Resolution should be high as possible. It depends on the number of bits in the digital input applied to DAC. Higher the number of bits, higher is the resolution.

Monotonocity: In an ideal D/A converter, the analogue output should increase by an identical step size for every one-LSB increment in the digital input word or A D/A converter is considered as monotonic if its analogue output either increases or remains the same but does not decrease as the digital input code advances in one-LSB steps.

Settling time: The settling time is the time period that has elapsed for the analogue output to reach its final value within a specified error band after a digital input code change has been effected. General-purpose D/A converters have a settling time of several microseconds, while some of the high-speed D/A converters have a settling time of a few nanoseconds.

DIFFERENT TYPES OF ADC'S

In electronics, an Analog to Digital Converter (ADC) is a device for converting an analog signal (voltage, current etc.) to a digital code, usually binary. In the real world, most of the signals sensed and processed by humans are analog signals.
Analog to Digital conversion is the primary means by which analog signal are converted into digital data that can be processed by computers for various purposes.

It accepts an analog input voltage Va and produces an output binary word d1, d2, d3….dn. Where d1 is the most significant bit and dn is the least significant bit.

In A/D conversion, there are two main steps of process:

1. Sampling and Holding
2. Quantization

In order to be able to perform digital signal processing on natural signals that are analog in nature, they must first be sampled and quantized into digital form.

TYPES OF A to D CONVERTOR:

1) Direct type
   i) Parallel comparator (Flash) ADC ii) Counter ADC iii) Successive Approximation ADC
   iv) Servo tracking ADC

Integrated type ADCs perform conversion in an indirect manner by first changing the analog input signal to linear function of time or frequency and then to a digital code.

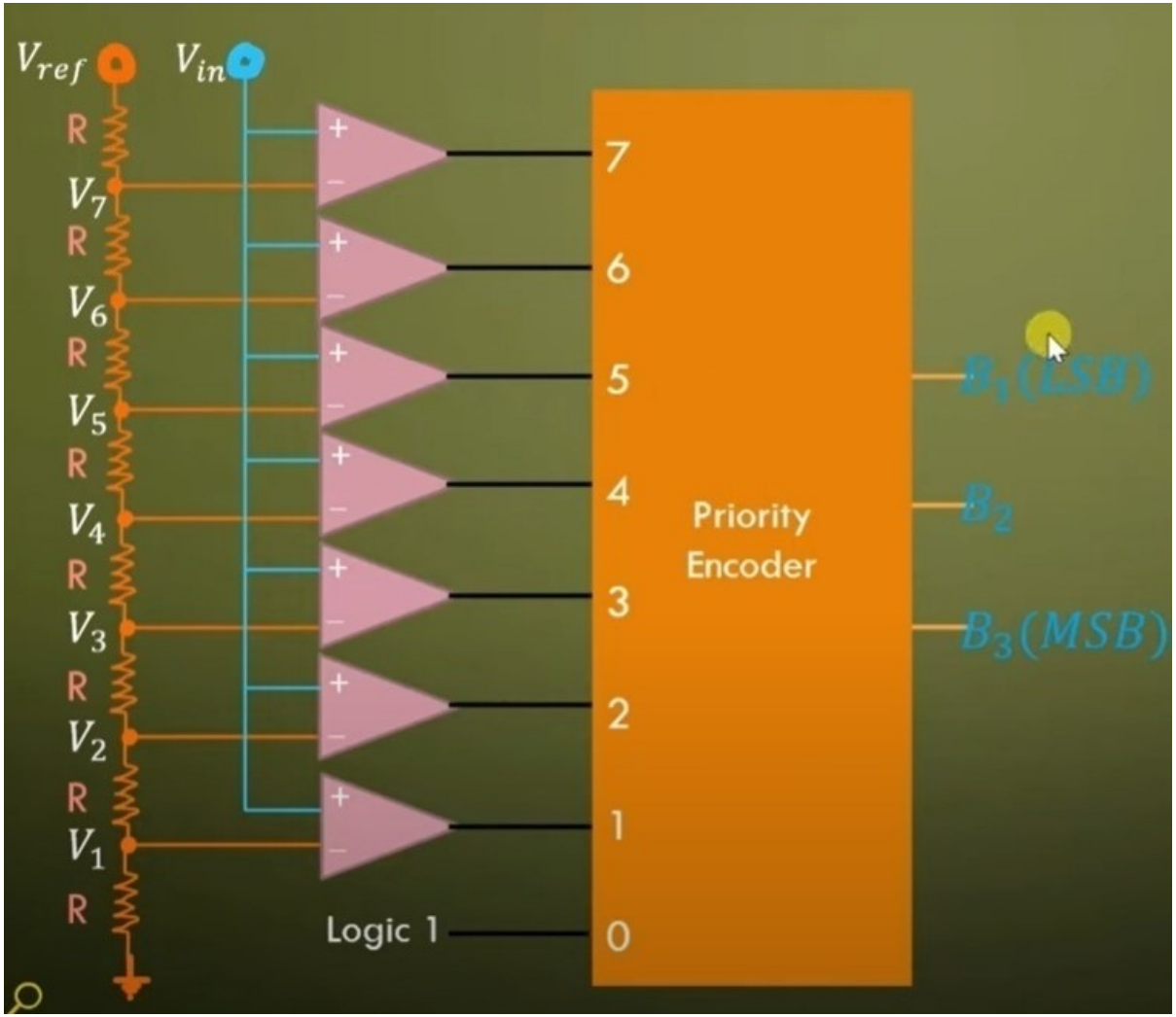
2) Integrating type of ADC
   i) Charge balancing ADC ii) Dual slope ADC

FLASH (COMPARATOR) TYPE CONVERTER: Fastest analog to Digital converter

A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, 2N - 1, doubles with each additional bit, requiring a large, expensive circuit.

A Flash ADC (also known as a direct conversion ADC) is a type of analog-to- digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors. The output of these comparators is generally fed into a digital encoder which converts the inputs into a binary value.

Also called the parallel A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.



Circuits consists of
2^N-1 comparators
2^N resistors for voltage divider network
One priority Encoder

$$V_1 = V_{ref}\left[\frac{R}{8R}\right] = \frac{V_{ref}}{8}$$

$$V_2 = V_{ref}\left[\frac{2R}{8R}\right] = \frac{2V_{ref}}{8}$$

...

$$V_7 = V_{ref}\left[\frac{7R}{8R}\right] = \frac{7V_{ref}}{8}$$

In Priority encoder, here priority is given in descending order. So, highest (7) and lowest (0) priority is given.

The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

The **working** of a 3-bit flash type ADC is as follows:

- The **voltage divider network** contains 8 equal resistors. A reference voltage V_R is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of $\frac{V_R}{8}$.

- The external **input voltage** V_i is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.

- At a time, all the comparators compare the external input voltage V_i with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator **parallelly**.

- The **output of the comparator** will be '1' as long as V_i is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, V_i is less than or equal to the voltage drop present at the respective other input terminal.

- All the outputs of comparators are connected as the inputs of **priority encoder**. This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.

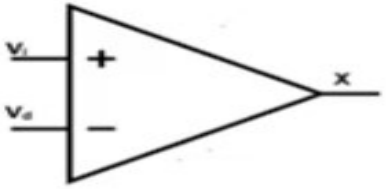
- Therefore, the output of priority encoder is nothing but the binary equivalent (**digital output**) of external analog input voltage, V_i.

The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

- Consist of a series of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which produces a binary output.

Flash type ADC:

- Operating conditions:
- $V_i > V_d$; X = 1
- $V_i < V_d$; X = 0
- $V_i = V_d$; X = previous state



- Encoder compares the code resulting from the comparators into binary code.

Flash type, Priority encoder is used, It takes highest priority output coming from comparator and convert it to digital output.
X7 is highest priority, X0 is lowest priority, if X7 to X0 all are high (1). Encoder consider X7 remaining outputs are neglect, X7 convert to digital.
If X3, X2 are high, remaining outputs are low, encoder convert X3 to digital, neglect X2. X3 is high priority than X2.

Truth Table for Flash ADC:

X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	1	1	1	0	1	0
0	0	0	0	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

Flash type ADC:

- Advantages:
- High speed (Simultaneous)
- Conversion time is less
- Conversion time is limited only by the speed of comparator and c the priority encoder.
- Disadvantages:
- Number of comparators required double for each added bit.
- The larger value of n, the more complex is the priority encoder.

- Simplest A/D
- Fastest A/D
- Expensive
- 8 –opamps
- 8-3 Priority Encoder
- V_R divides equally

- It is fastest ADC (Giga Samples per second)
- Useful with large bandwidth input

- High Power consumption
- Limited resolution (Up to 8 bits)
- Large size due to comparator (for 8 bits 255 comparator)
- With more comparator need of higher accurate matching network

The conversion time is T_{clk}

Applications of Flash ADC

- Satellite Communication
- RADAR processing
- Oscilloscope

Problems:

- A 8-bit ADC outputs all 1's when Vi = 5.1V. Find its
  (a) Resolution (b) digital output when vi = 1.28V
- **Solution**:
- (a) Resolution = $2^8 = 256$
- Resolution in volts = $5.1/(2^8-1) = 20mV/LSB$
- (b) For 1.28V input digital output can be calculated as,

$$D = \frac{1.28\ V}{20\ mV/LSB} = 64\ LSBs$$

$$\text{Digital Output} = \frac{2^N \times \text{Analog Input Voltage}}{\text{Reference Voltage}}$$

N = Number of Bits

The binary equivalent of 64 is $0100\ 0000_2$

Problem:

- What output voltage will be produced by a 4bit D/A converter whose output range is 0V to 10V and whose input binary is 0110 ?
- **Solution:**

$$\text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{10}{2^4 - 1} = 0.667\ V;$$

$$V_o = 0.667 \times (0110)_2 = 0.667 \times 6 = 4\ V$$

In flash ADC number of comparator required is double for add of each bit. This problem is over com by Counter type ADC.

Counter Type A/D (ADC Using DAC):

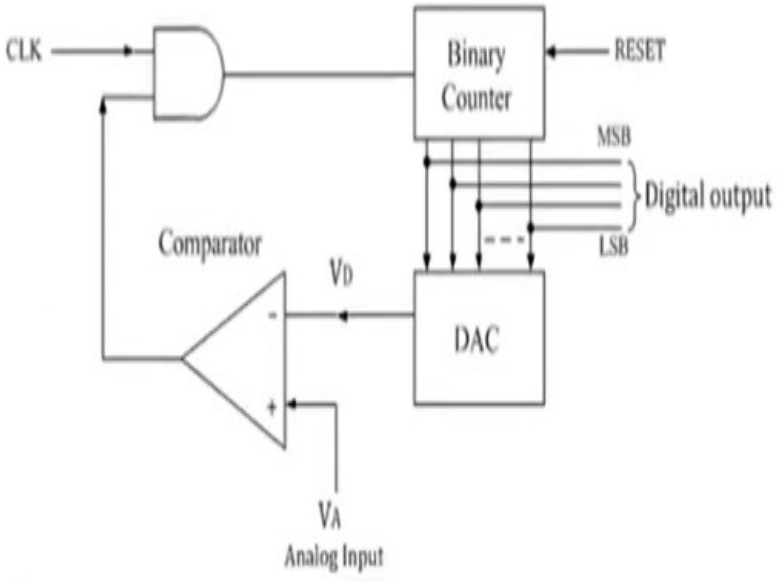
- Basic principle: The linear ramp can be produced by connecting the output of a counter to the input of a DAC.

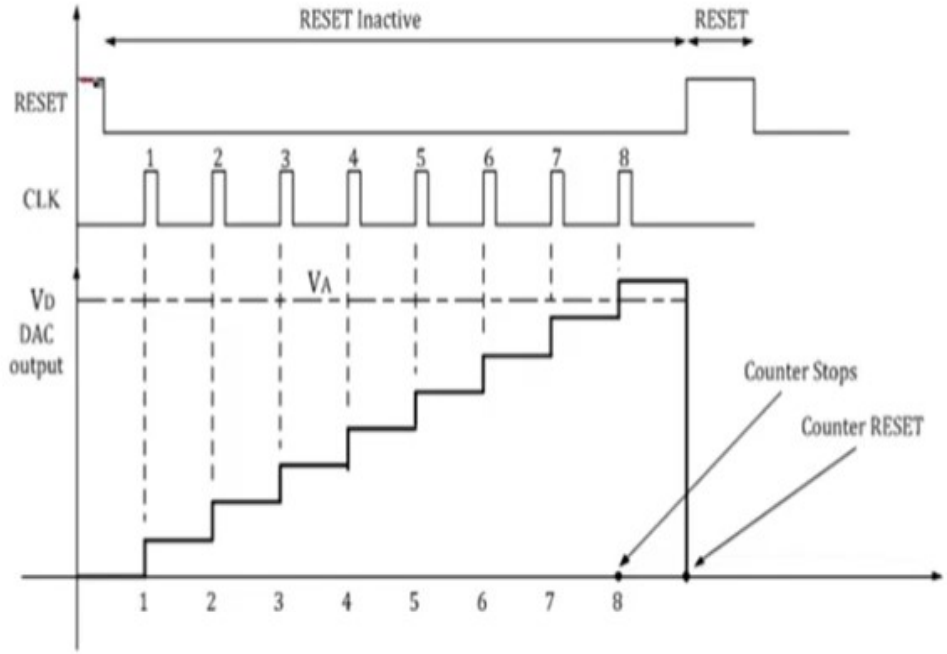
Operation:

- The n-bit binary counter is initially set to 0 by usin reset command.
- Therefore the digital output is zero and VD =0V.
- The clock pulses are allowed to go through AND gate and are counted by the binary counter.
- The D to A converter (DAC) converts the digital output to an analog voltage and applied as the inverting input to the comparator.

- The number of clock pulses increases with time and the analog input voltage VD is a rising staircase waveform.
- The counting will continue until the DAC output VD > VA
- Then the comparator output becomes low and this disables the AND gate from passing the clock.
- The counting stops at the instance VA< VD, and at that instant the counter stops its progress and the conversion is said to be complete.

COUNTER TYPE A/D CONVERTER:





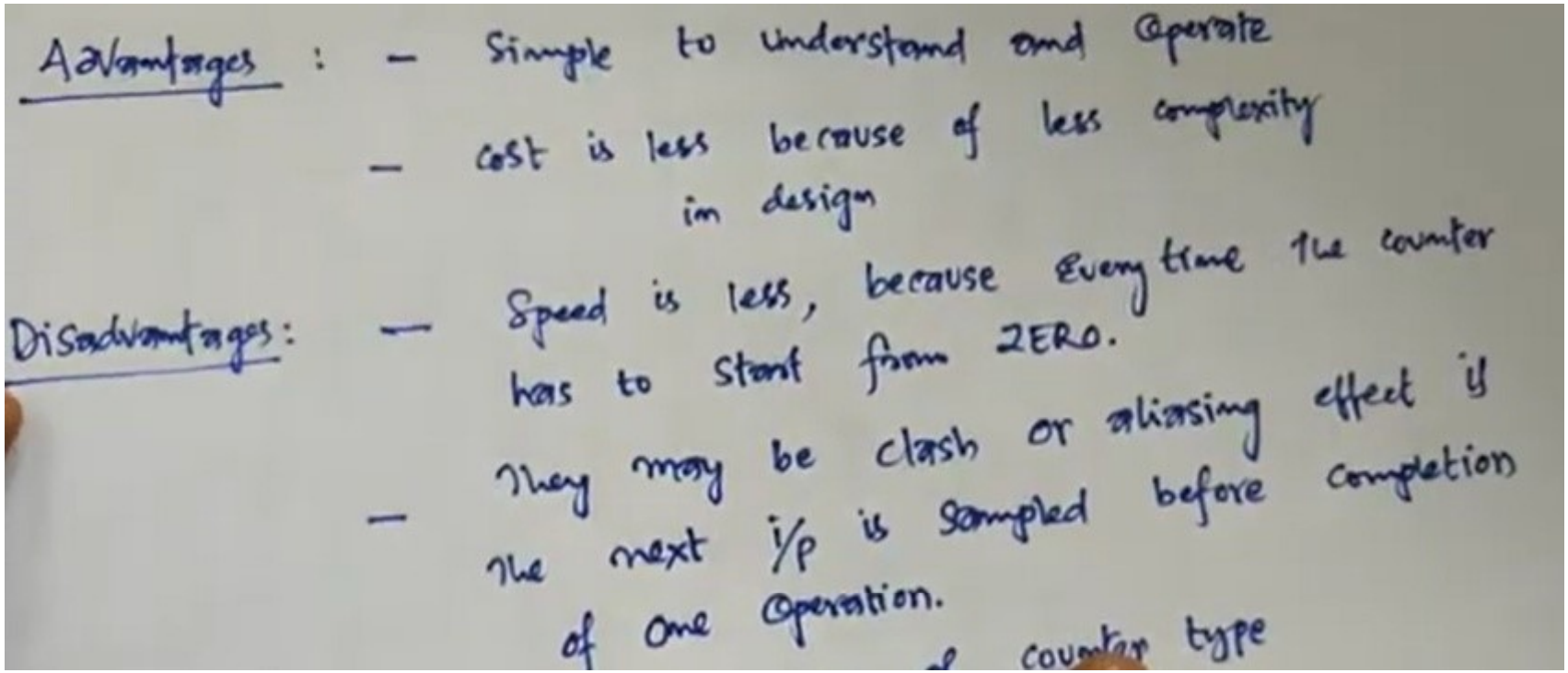
The counter is reset to zero count by reset pulse. After releasing the reset pulse the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time.

The binary word representing this count is used as the input of a D/A converter whose output is a stair case. The analog output Vd of DAC is compared to the analog input Va by the comparator. If Va>Vd the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When Va<Vd the output of the comparator becomes low and the AND gate is disabled. This stops the counting we can get the digital data.

The counter type ADC mainly consists of 5 blocks: Clock signal generator, Counter, DAC, Comparator and Control logic.

The **working** of a counter type ADC is as follows:

- The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it received the start commanding signal.
- The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. This output of the counter is applied as an input of DAC.
- **DAC** converts the received binary (digital) input, which is the output of counter, into an analog output. Comparator compares this analog value, V_a with the external analog input value V_i.
- The **output of comparator** will be '**1**' as long as V_i is greater than V_a. The operations mentioned in above two steps will be continued as long as the control logic receives '1' from the output of comparator.
- The **output of comparator** will be '**0**', when V_i is less than or equal to V_a. So, the control logic receives '0' from the output of comparator. Then, the control logic disables the clock signal generator so that it doesn't send any clock pulse to the counter.
- At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value V_i.



Conversion time Ts > = (2^N-1) X T

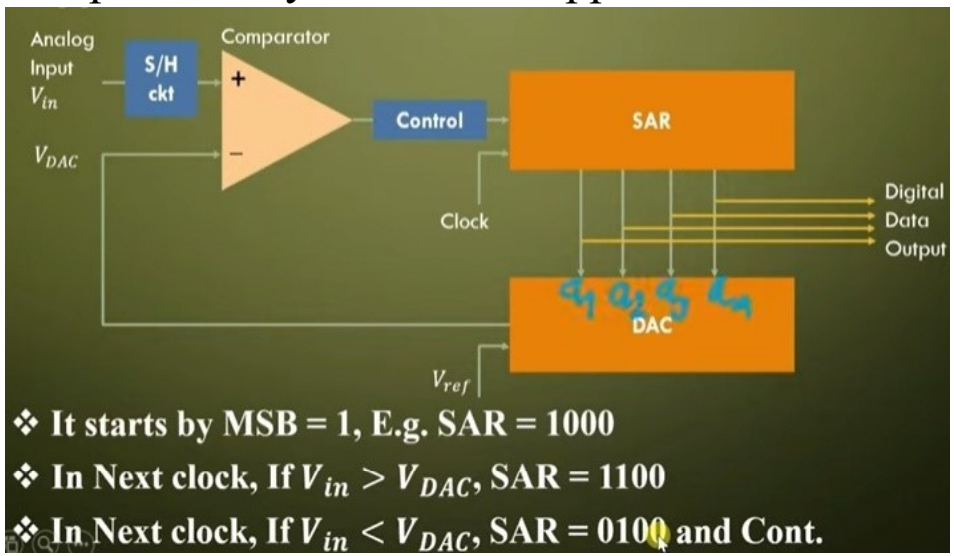
Counter type ADC: The conversion time is **$(2^n - 1)\ T_{clk}$**, where n is the number of bits in the ADC. Counter type ADCs use a linear search and a DAC.

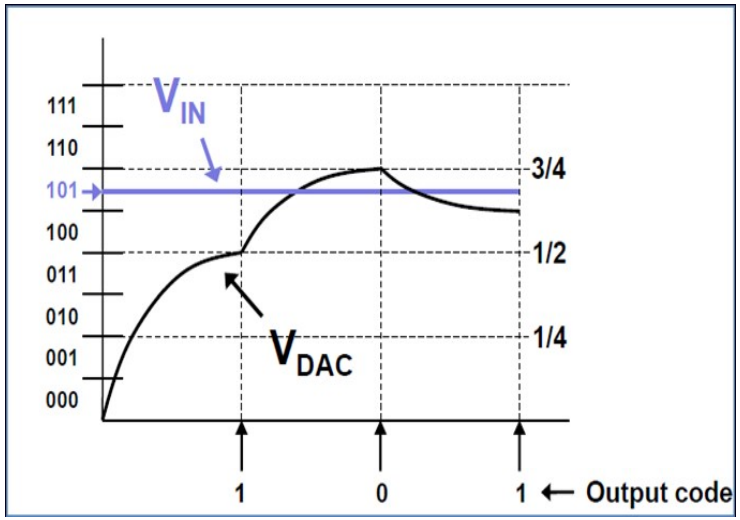
Counter Type A/D:

- Advantages:
  - Simple construction.
  - Easy to design and less expensive.
  - Speed can be adjusted by adjusting the clock frequency.
  - Faster than dual slope type ADC.
- Disadvantage:
  - Conversion time depends on input signal amplitude.

Successive-approximation ADC:

Counter ADC, takes more time to convert the digital if input is larger value. To overcome this problem by Successive approximation ADC





- Works with very efficient code searching strategy called **Binary Search.**
- N Bit conversion completes in n clock cycles.

- Circuit uses Successive approximation register (SAR) , DAC & comparator.
- External clock sets the internal timing parameters
- SOC — Starts the process
- EOC — activated after conversion process finish.

- The SOC initiates the process of search
- The SAR sets - MSB bit (MSB =1)
- Then corresponding V_D generates by DAC.
- If $V_A > V_D$, then Next significant bit will be set (1)
- If $V_A < V_D$, then MSB = 0 , next significant bit will be set to 1 by the SAR and then the process will be repeated.
- The comparator changes its state whenever the DAC crosses VA and this activates the EOC .

The successive approximation ADC mainly consists of 5 blocks: Clock signal generator, Successive Approximation Register (SAR), DAC, comparator and Control logic.

The **working** of a successive approximation ADC is as follows:

- The **control logic** resets all the bits of SAR and enables the clock signal generator in order to send the clock pulses to SAR, when it received the start commanding signal.
- The binary (digital) data present in **SAR** will be updated for every clock pulse based on the output of comparator. The output of SAR is applied as an input of DAC.
- **DAC** converts the received digital input, which is the output of SAR, into an analog output. The comparator compares this analog value V_a with the external analog input value V_i.
- The **output of a comparator** will be '1' as long as V_i is greater than V_a. Similarly, the output of comparator will be '0', when V_i is less than or equal to V_a.
- The operations mentioned in above steps will be continued until the digital output is a valid one.

The digital output will be a valid one, when it is almost equivalent to the corresponding external analog input value V_i.

- **Advantages:**

  1 Conversion time is very small.

  2 Conversion time is constant and independent of the amplitude of the analog input signal VA.

- **Disadvantages:**

  1 Circuit is complex.

  2 The conversion time is more compared to flash type ADC.

The conversion time is $\mathbf{n\ T_{clk}}$

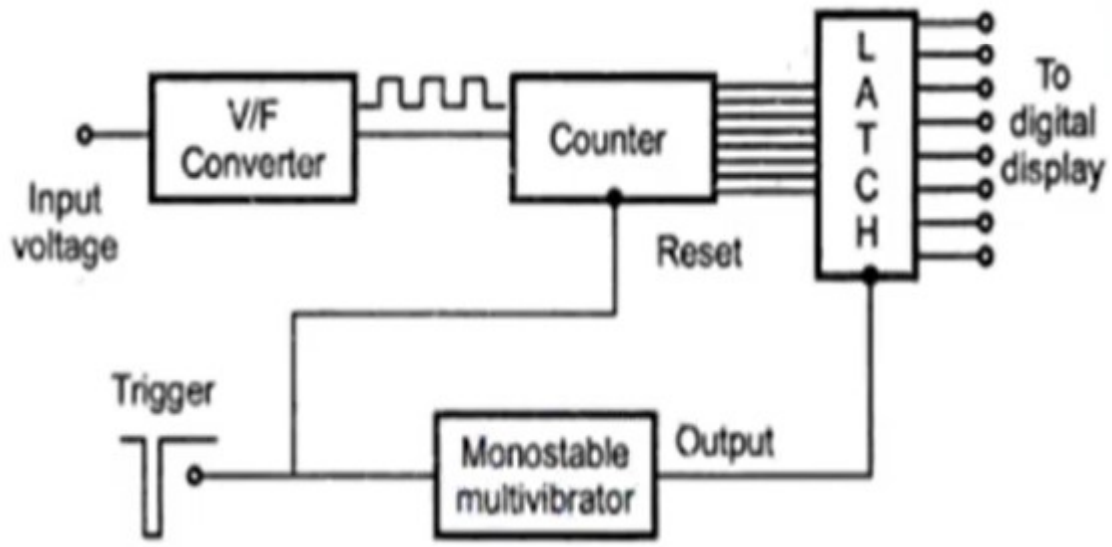
Charge balancing ADC:

Principle is to first convert the input signal into a frequency using a voltage to frequency (V/F) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input.

The main advantage of these converters is it is possible to transmit frequency even in noisy environment or in isolated form.

Limitation: Output of V to F converter depends on RC product whose value depends on temperature and time.

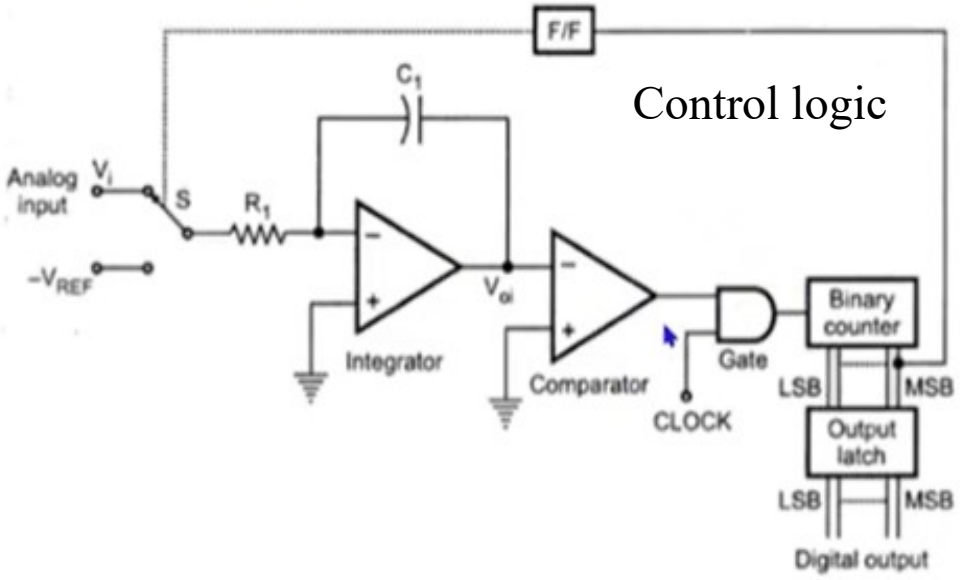
This drawback is overcome by dual slope conversion.



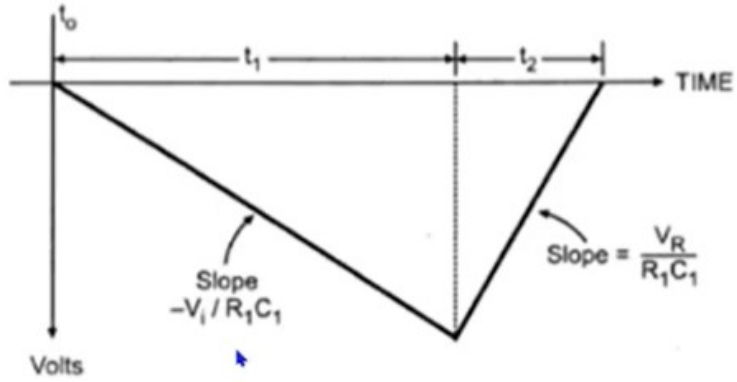
Dual Slope ADC:

High accurate ADC

- Indirect method of A/D Conversion.
- Ref voltage is converted into time periods by an integrator & then measured by counter.
- Speed of conversion is slow. But accuracy is high.
- Ramp generator input switched between V_i and a negative ref voltage – V_{ref}



Dual slope A/D converter



Integrator output voltage

When MSB is logic '1' the negative reference voltage is connected to the ramp generator.

- When MSB is '0' , the voltage being measured is connected to the ramp generator input.

An integrating ADC (also dual-slope ADC) shown in fig applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.

The dual slope ADC mainly consists of 5 blocks: Integrator, Comparator, Clock signal generator, Control logic and Counter.

The **working** of a dual slope ADC is as follows:

- The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it is received the start commanding signal.
- Control logic pushes the switch **sw** to connect to the **external analog input voltage** V_i, when it is received the start commanding signal. This input voltage is applied to an integrator.
- The output of the **integrator** is connected to one of the two inputs of the comparator and the other input of comparator is connected to ground.
- **Comparator** compares the output of the integrator with zero volts (ground) and produces an output, which is applied to the control logic.
- The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. It produces an overflow signal to the control logic, when it is incremented after reaching the maximum count value. At this instant, all the bits of counter will be having zeros only.
- Now, the control logic pushes the switch **sw** to connect to the **negative reference voltage** $-V_{ref}$. This negative reference voltage is applied to an integrator. It removes the charge stored in the capacitor until it becomes zero.
- At this instant, both the inputs of a comparator are having zero volts. So, comparator sends a signal to the control logic. Now, the control logic disables the clock signal generator and retains (holds) the **counter value**. The counter value is proportional to the external analog input voltage.
- At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value V_i.

The dual slope ADC is used in the applications, where **accuracy** is more important while converting analog input into its equivalent digital (binary) data.

- When MSB is '0' , the voltage being measured is connected to the ramp generator input.

When MSB is logic '1' the negative reference voltage is connected to the ramp generator.

- At time t=0, analog switch S is connected to the analog input voltage Vi, so that the analog input voltage integration begins, the output of integrator is given as,

$$V_{oi} = \frac{-1}{R_1 C_1} \int_0^t V_i \, dt$$

$$= \frac{-V_i \, t}{R_1 C_1}$$

- R_1C_1 is time constant & V_i is constant.
- At the end of 2^N clock periods MSB goes high.
- So, output of f/f goes high, which causes the switch S to be switched from V_i to $-V_R$
- Therefore, integrator output is +ve.
- When o/p reaches to 0, comparator o/p goes low.
- Which disables the AND gate, & counter stops

- The charge voltage equal to discharge voltage,

$$\frac{V_i t_1}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$V_i t_1 = V_R t_2$$

$$\boxed{t_2 = \frac{V_i t_1}{V_R}}$$

$$digital\ output = \left(\frac{Counts}{second}\right) t_2$$

$$digital\ output = \left(\frac{Counts}{second}\right) \frac{V_i t_1}{V_R}$$

Dual Slope ADC:

❖ Conversion time does not depends on R and C, so it gives very accurate conversion. Also this circuit is independent on temperature as output does not depends on R and C.

- Advantages:
  - It is highly accurate.
  - Cost is low.
  - It is immune to temperature caused variations in R_1 & C_1
- Disadvantage:
  - Speed of conversion is low.

Dual slope ADC: The conversion time is $(2^n+1)\ T_{clk}$.

Problems:

- For a particular dual slope ADC, t_1 is 83.33ms and the reference voltage is 100mV calculation t2 if (i) Vi = 100mv and ii)200mV

$$t_2 = \left(\frac{V_i}{V_R}\right) t_1$$

i) $$t_2 = \left(\frac{100}{100}\right)(83.33) = 83.33 \text{ ms}$$

ii) $$V_i = 200 \text{ mV}$$

$$t_2 = \left(\frac{200}{100}\right)(83.33) = 166.6 \text{ ms}$$

Problems:

- For a 3-bit weighted resistor DAC, calculate the resistor values if the smallest resistor is 25Ω.
- Solution:
- Given 2R = 25 Ω
- R = 12.5 Ω
- Second resistor = 4R = 50 Ω
- Third resistor = 8R = 100 Ω

Problems:

1. Measure the output voltage produced by a DAC whose output range is 0-10V and whose input binary number is (I) 10 (II) 0110 (III) 10111100 (IV)1000

olution

(i) $V_o = 10\ \text{V}\left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5\ \text{V}$

ii) $V_o = 10\ \text{V}\left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right)$

$= 10\left(\frac{1}{4} + \frac{1}{8}\right) = 3.75\ \text{V}$

ii) $V_o = 10\ \text{V}\,(1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5$
$+ 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8)$
$= 10\ \text{V}\,(1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34\ \text{V}$

2. The LSB of 10 bit DAC 20 mV.

- What is its percentage of resolution
- What is its full scale range?

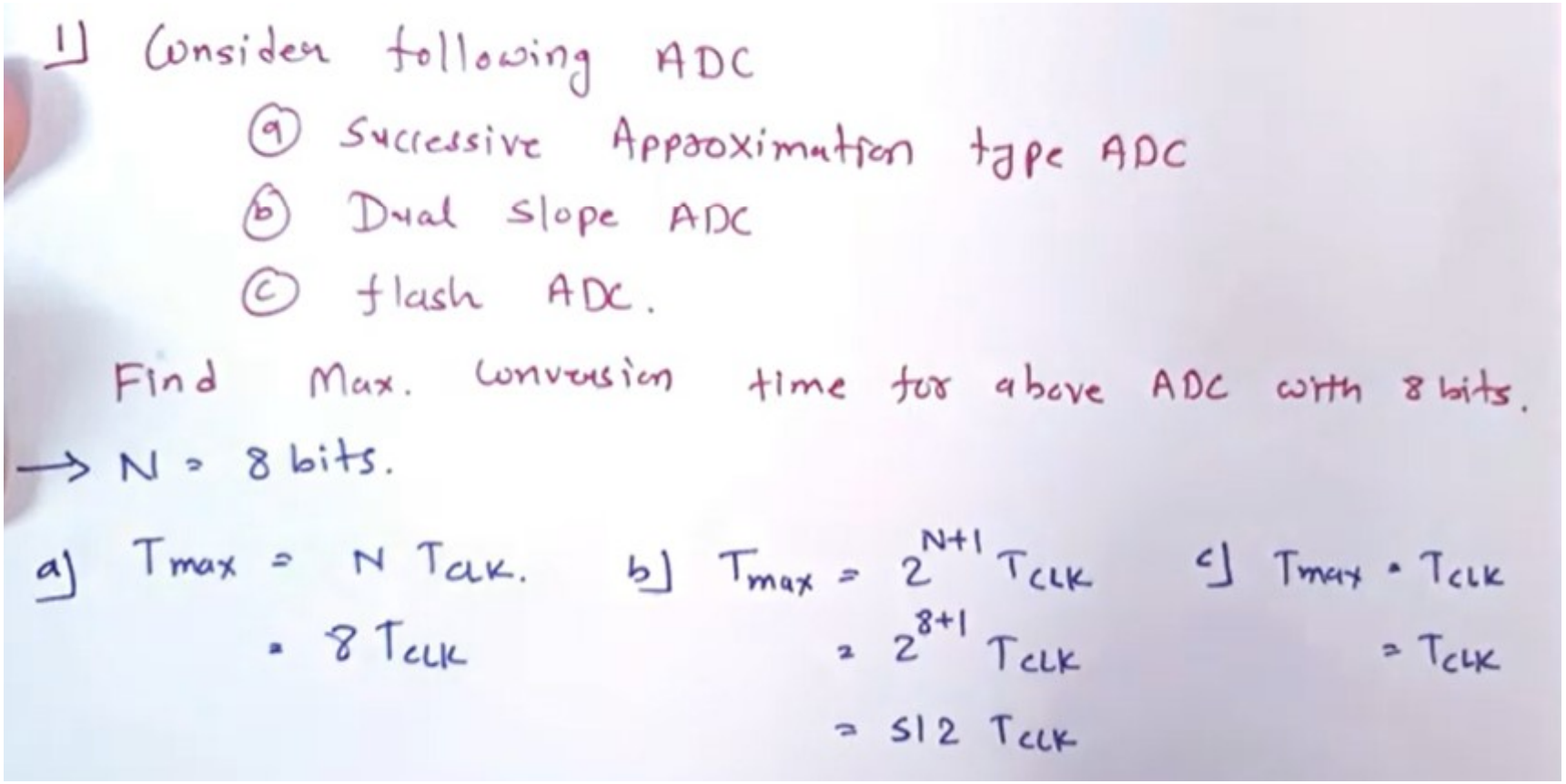
What is the output voltage for input 1011001101

The resolution of a 4 bit counting ADC is 0.5 V. For an analog input of 6.6V. The digital output of ADC will be---------

Sol: N=4, resolution = 0.5v, vin=6.6v

Number of steps = Vin/ resolution = 6.6v/ 0.5v =13.2

13 equivalent digital output =1101



3] A 12 bit ADC is Operating with Clock of 1μsec Clock period & total Conversion time is seen to be 14 μsec. The ADC must be

(a) Flash ADC
(b) Counter type [Note take Circuit delay = 2μsec]
(c) Successive Approximation type
(d) Dual Slope

Flash ADC $T_{max} = T_{clk} = 1\mu sec + 2\mu sec = 3\mu sec$

Counter ADC $T_{max} = (2^N - 1) T_{clk.} = (2^{12} - 1) 1\mu sec + 2\mu sec$
$= 4095 + 2 = 4097\ \mu sec$

Successive App. ADC $T_{max} = N T_{clk}$
$= 12 \times 1\mu sec + 2\mu sec = 14\ \mu sec.$

Dual Slope ADC $T_{max} = 2^{N+1} T_{clk} + 2^{13} T_{clk} + 2\mu sec$

The conversion time of different types of analog-to-digital converters (ADCs) depends on the type of ADC and the number of bits in the ADC:

Counter type ADC: The conversion time is $\mathbf{(2^n - 1)\ T_{clk}}$, where n is the number of bits in the ADC. Counter type ADCs use a linear search and a DAC.

Successive approximation ADC: The conversion time is $\mathbf{n\ T_{clk}}$. Successive approximation ADCs use a ring counter and binary search. 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones generally take several microseconds.

Flash type ADC: The conversion time is $\mathbf{T_{clk}}$.

Dual slope ADC: The conversion time is $\mathbf{(2^n+1)\ T_{clk}}$.

Example 3.25.4 *Find out stepsize and analog output for 4-bit R-2R ladder DAC when input is 1000 and 1111. Assume* $V_{ref} = +5$ *V.*

Solution : For given DAC, n = 4, $V_{oFS} = +5$ V

Resolution = $V_{oFS} / 2^n - 1 = 5 / 2^4 - 1 = 1/3$ V / LSB

V_o = Resolution × D

For = Decimal of $(1000)_2 = 8$

$V_o = 1/3 \times 8 = 2.6667$ V

For D = Decimal of $(1111)_2 = 15$

$V_o = 1 / 3 \times 15 = 5$V.

Example 3.25.5 *A 12-bit DAC has a step size of 8 mV. Determine the full scale output voltage and percentage resolution. Also find the output voltage for the input of 010101101101?*

Solution : For 12-bit DAC, step size is 8 mV.

$V_{oFS} = 8\text{mV} \times 2^{12} - 1 = 32.76$ V 8mV

% Resolution = 8mV / 32.76V × 100 = 0.02442 %

The output voltage for the input 010101101101 is = 8 mV × $(1389)_{10} = 11.112$ V

Design a 4 bit R-2R ladder network, determine the size of each step if R = 10 kΩ, R_f = 20 kΩ and V_{CC} = ± 15 V. Calculate the output voltage for D_o = 1, D_1 = 0, D_2 = 1 and D_3 = 1 if bit '1' applied as 5 V and bit 'O' applied as 0 V.

The output voltage for DAC shown in Fig. 3.25.12 is given by

$$V_o = \frac{V_R \times 20\,K}{10\,K}\left(D_3\,2^{-1} + D_2\,2^{-2} + D_1\,2^{-3} + D_0\,2^{-4}\right)$$

$$V_{OFS} = \frac{V_R \times 20\,K}{10\,K}\left(1\times2^{-1} + 1\times2^{-2} + 1\times2^{-3} + 1\times2^{-4}\right)$$

$$= 5 \times 2\ (0.9375)$$

$$= \mathbf{9.375\ V}$$

$$\text{Resolution} = \text{Size of each step} = \frac{V_{OFS}}{2^n - 1} = \frac{9.375}{2^4 - 1} = \mathbf{0.625\ V}$$

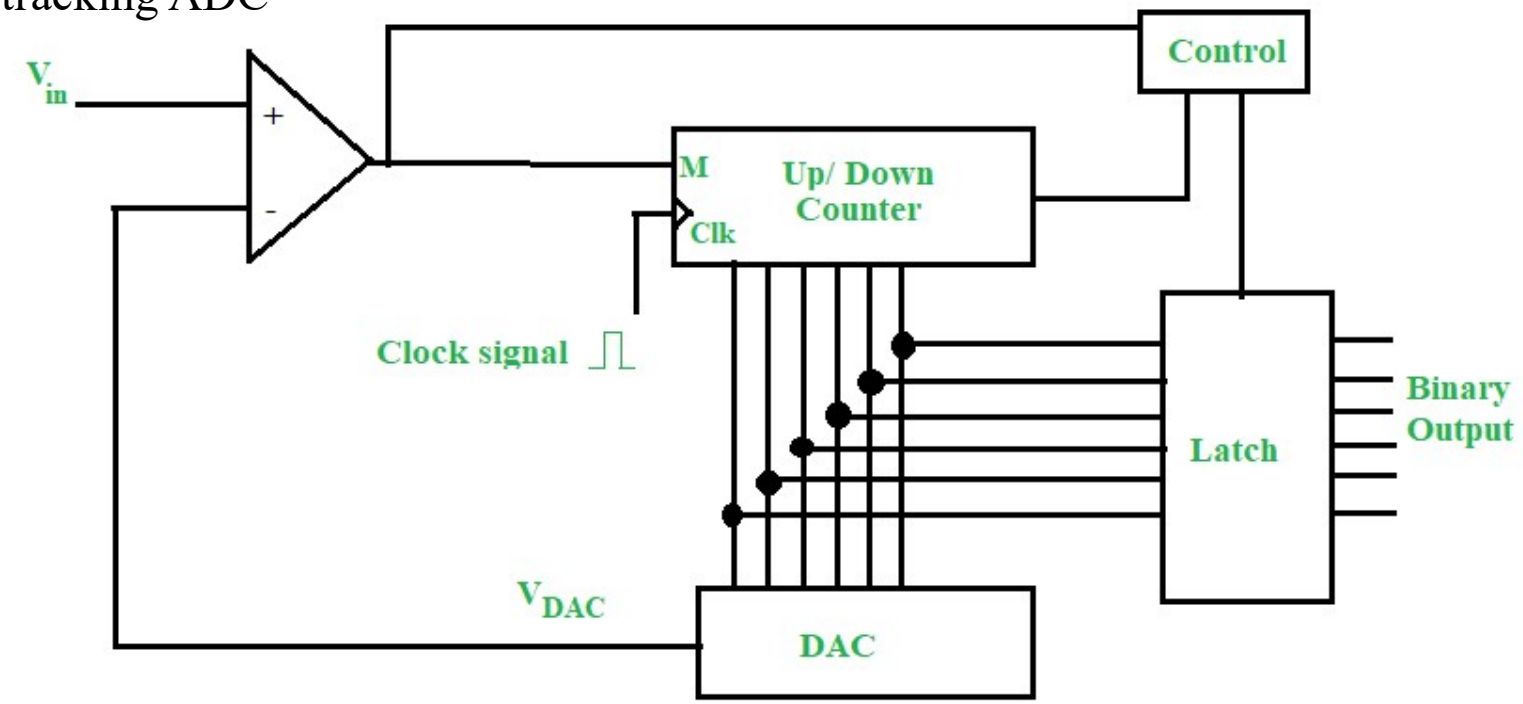
Output voltage for : D_0 = 1, D_1 = 0, D_2 = 1 and D_3 = 1

$$V_o = \text{Resolution} \times D \qquad \text{where D = Decimal of (1101) = 13}$$

$$= 0.625 \times 13$$

$$= \mathbf{8.125\ V}$$

Servo tracking ADC



The circuit of the tracking type is shown above. We have a comparator with inputs coming from Vin and from the output terminal of the DAC. This comparator's output is given to the up/down counter terminal M. External clock signal is also provided. When M = 1, the counter performs up-counting. When M = 0, the counter performs down-counting. The counter values are converted to appropriate decimal values by the Digital-to-Analog Converter (DAC) and this is again given back to the comparator as a feedback signal for continuous comparison. A latch is provided to retain the counter's final stage at the end of conversion. The latch is triggered by the control box.

Thanks for all